

Block Diagram

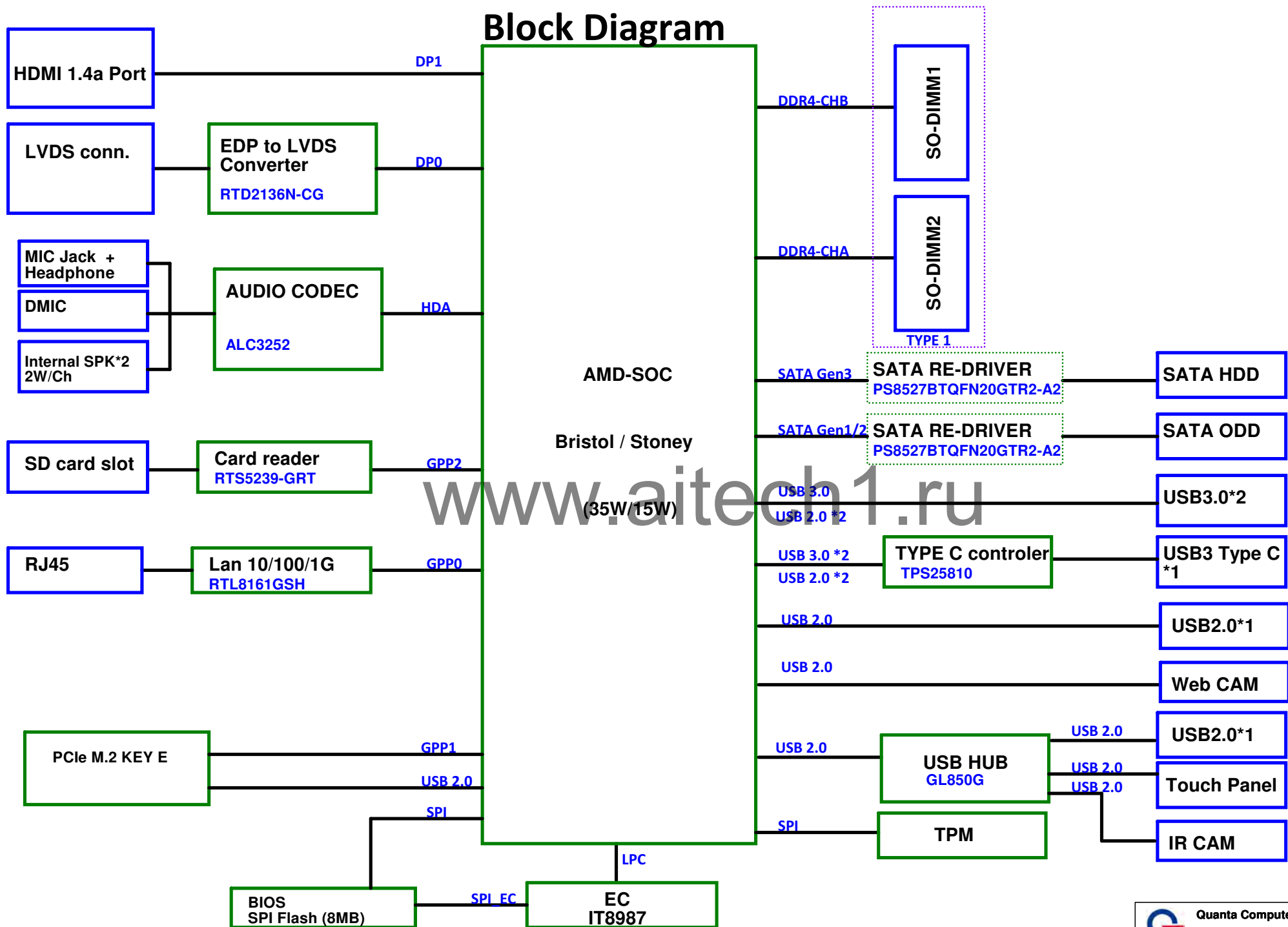


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POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
+VIN	+19V		Always
VCCRTC	+1.5V		Always
+3V	+3.3V	MAIN_ON1	S0
+3V_S3	+3.3V	S3_ON	S0~S3
+3V_S5	+3.3V	S5_LOAD_CODE	S0~S5
+3V_ALW	+3.3V	AC/DC Insert enable	Always (LDO)
+5V	+5V	MAIN_ON1	S0
+5V_S3	+5V	S3_ON	S0~S3
+5V_S5	+5V	S5_ON	S0~S5
+5V_ALW	+5V	AC/DC Insert enable	Always (LDO)
+3.3V_WLAN	+3.3V	EN_WLAN_PWR	S0~S5
+3.3V_LAN	+3.3V	LAN_PWR_ON	S0~S5
+VDDQ	+1.2V	S3_ON	S0~S3
+2.5V_S3	+2.5V	S3_ON	S0
+1.8V_S5	+1.8V	S5_ON	S0~S5
+1.8V	+1.8V	MAIN_ON2	S0
+VDDP_S5	+1.05V	S5_ON	S0~S5
+VDDP	+1.05V	S0_ON1_D	S0
+VDDCR_FCH_S5	+0.775V	S5_ON	S0~S5
CPU_CORE	~	VRON	S0
NB_CORE	~	VRON	S0
+12V	+12V	MAIN_ON1	S0
+SMDDR_VTERM	+0.6V	S3_ON	S3

Schematic "Value" Definition

Pavilion AMD Platform Phuket and Samui		DB/SI/PV Stage			MP	
By Value format	Description	Auto BOM Control	Phuket	Samui	Phuket	Samui
XX	Install	V	V	V	V	V
*XX	Non-Install	V				
BR@XX	Install AMD Bristol only	V	V		V	
ST@XX	Install AMD Stoney only	V		V		V
PROTO@XX	Install in pre-production only	V	V	V		
MP@XX	Install in MP only	V			V	V

***Board ID by manual control

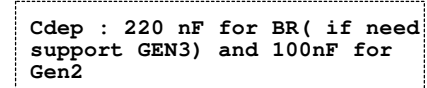


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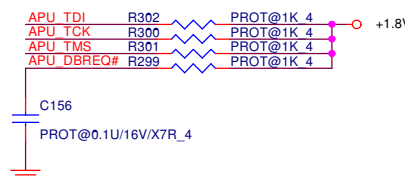
Project: HP-PHUKET

TitlePOWER STAGE & Bof-FUNCTION		RevC
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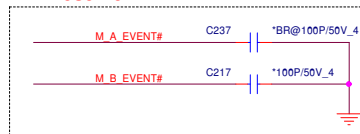
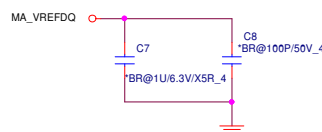
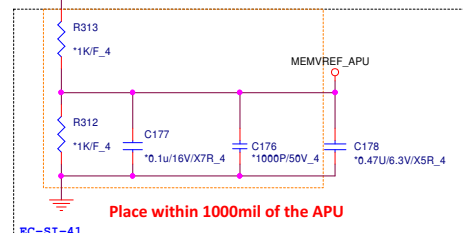
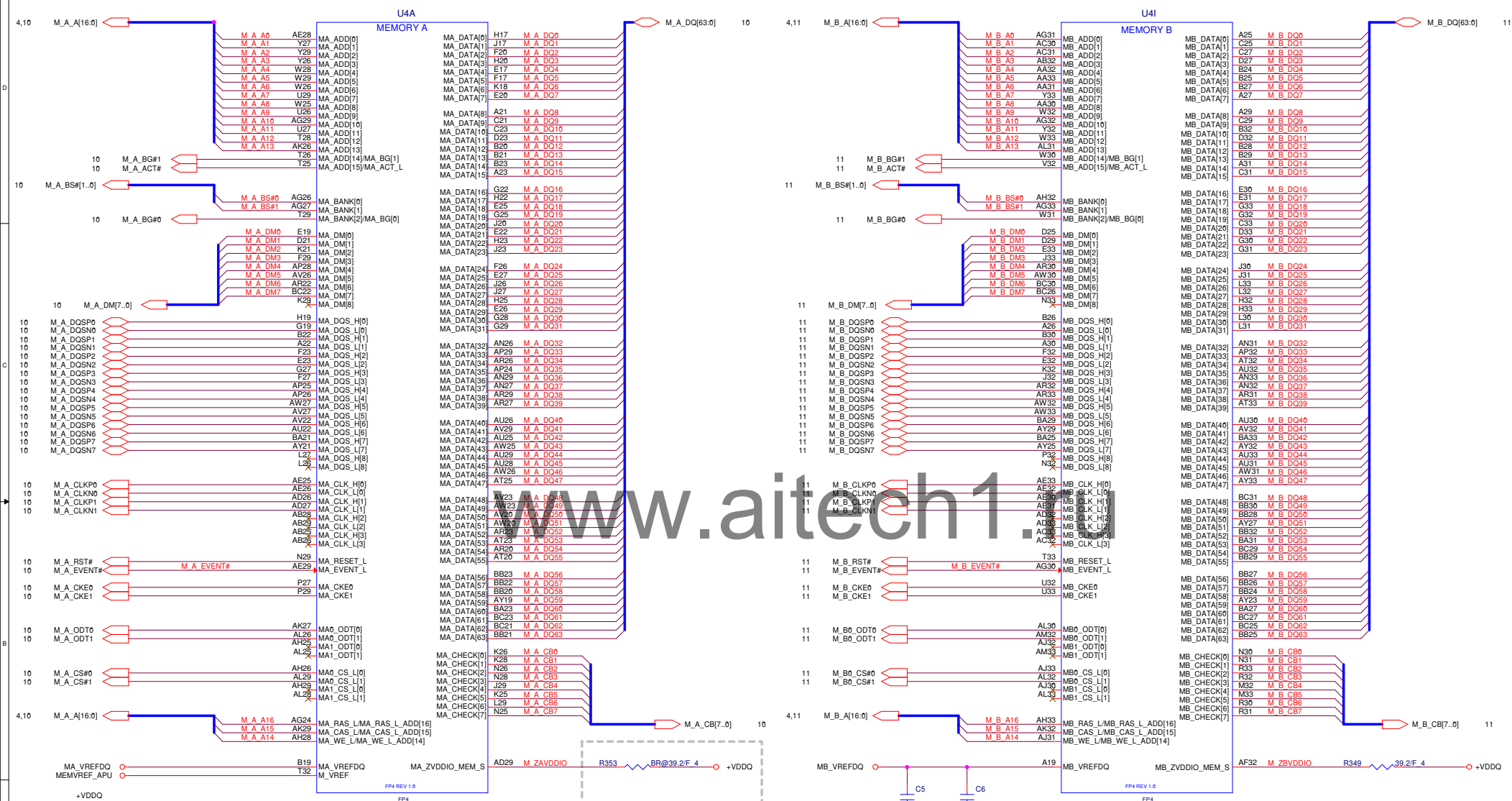
```
GPP:BR: support GEN3 (1.05V)
ST:support GEN2 (0.95V)
-->current GEN2 only.
```

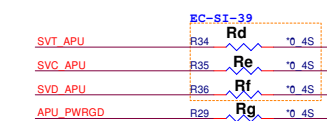
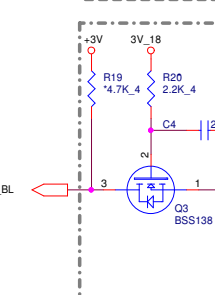
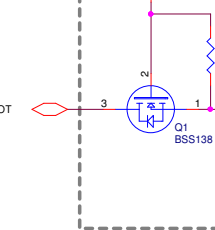
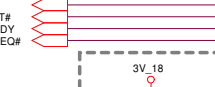
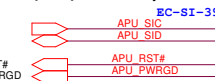
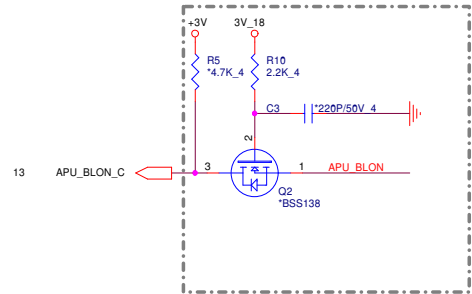
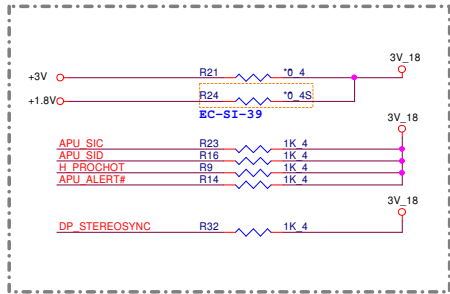
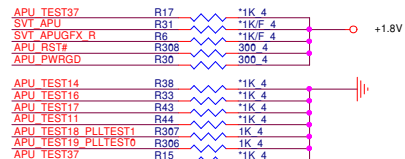
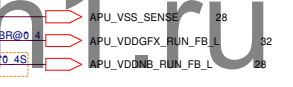
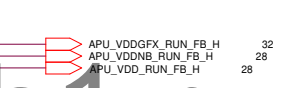
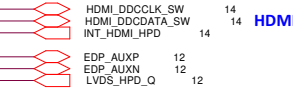
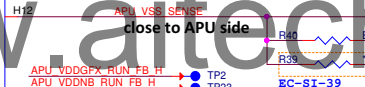
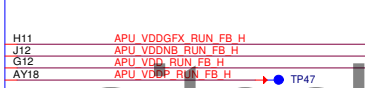
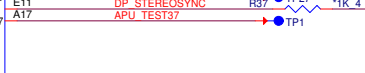
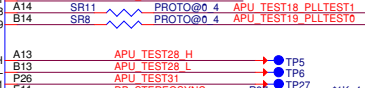
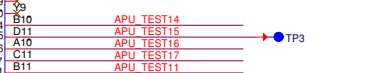
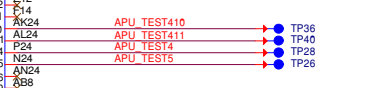
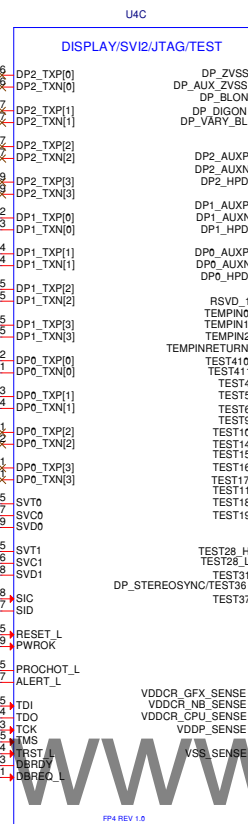
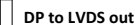


HDT+ Debug Connector

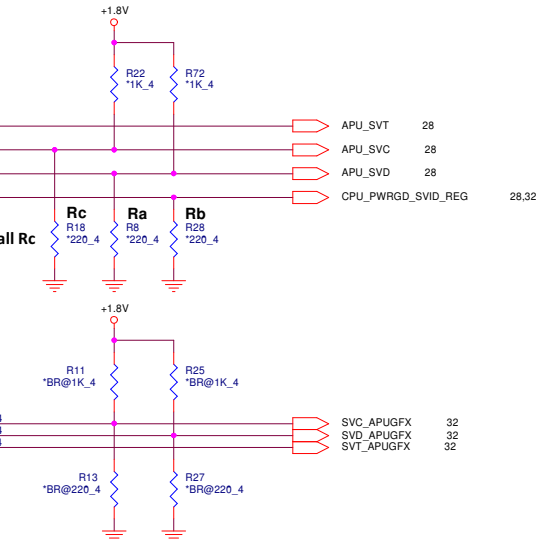


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Note:
To override VID, Remove Rd, Re, Rf, Rg, i
set VID via SVC & SVD option RES Ra, Rb



SVC/SVD

SVC	SVD	BOOT VOLTAGE
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

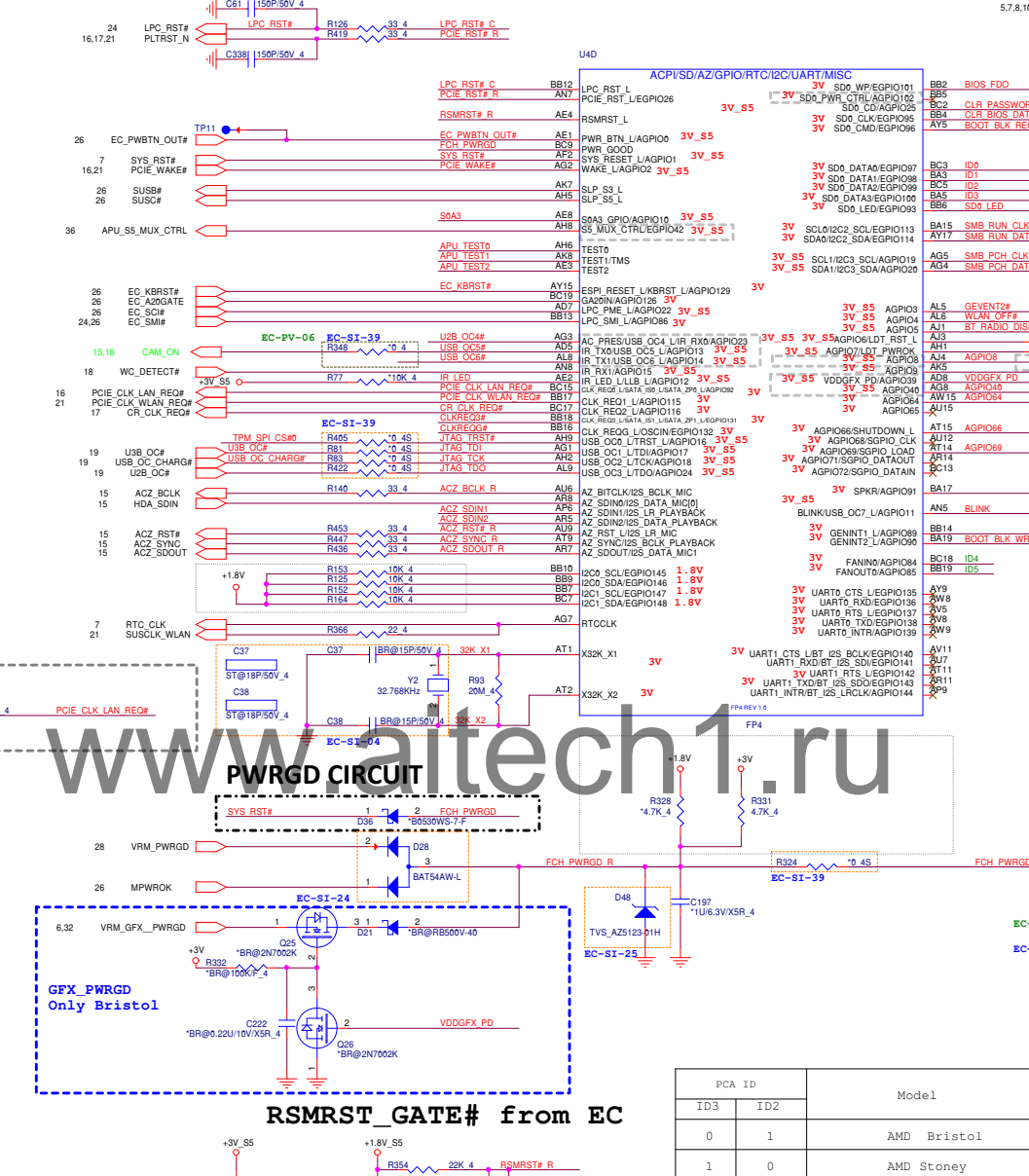
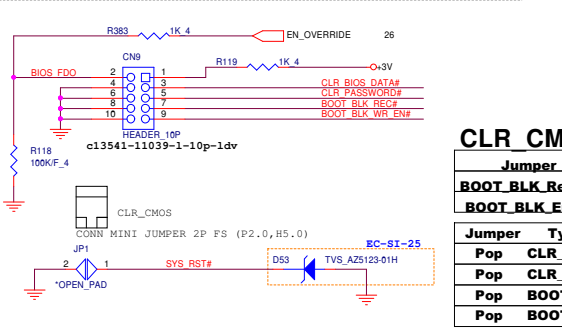
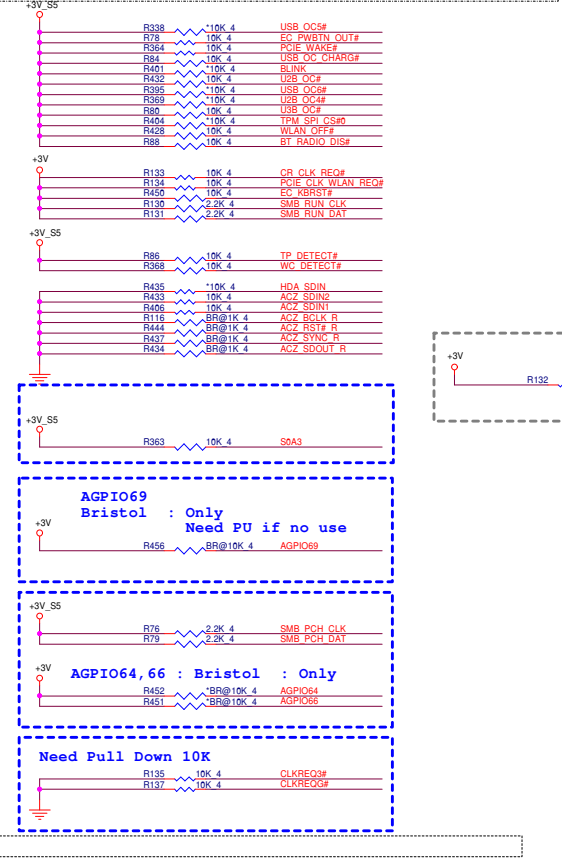


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Title			Display/SVI2/JTAG/Test Pin		
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NC,no install by default

TEST2	TEST1	TEST0	Description
0	0	0	FCH JTAG accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled



CLR CMOS

Jumper	Pre-production	Production
BOOT_BLK_Recovery	X	X
BOOT_BLK_Enable	O	X

Jumper	Type
Pop CLR BIOS_DAT	
Pop CLR PASSWD	
Pop BOOT_BLK_Recovery	
Pop BOOT_BLK_Enable	

EMI/ESD reserve

Board ID

Board REV	ID1	ID0	Model
0	0	0	All DB (EVT)
1	0	0	All SI (DVT)
0	1	0	PVT1
1	1	1	PVT2+
0	0	0	MVB, A
0	1	0	1st Major ECN
1	0	0	2nd Major ECN
1	1	1	3rd Major ECN

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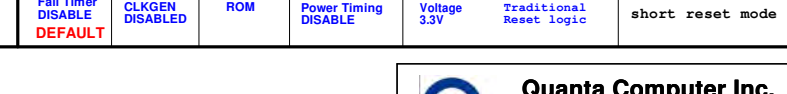
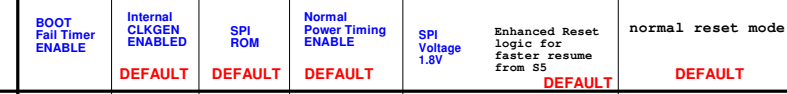
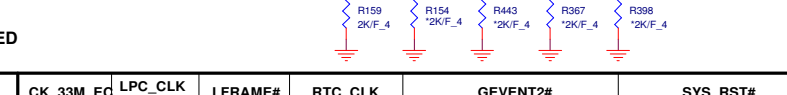
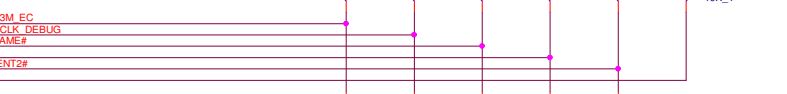
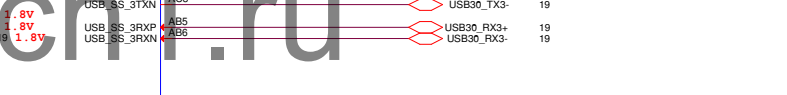
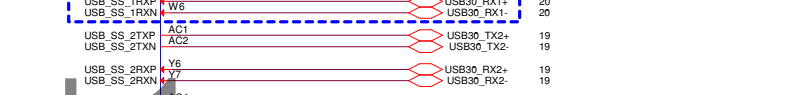
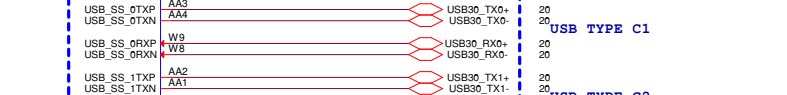
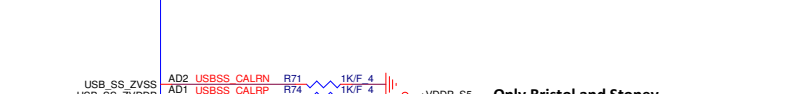
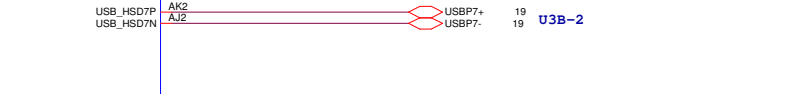
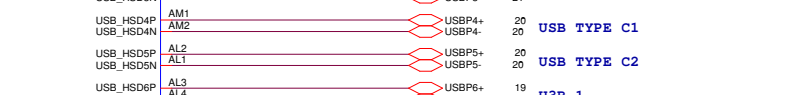
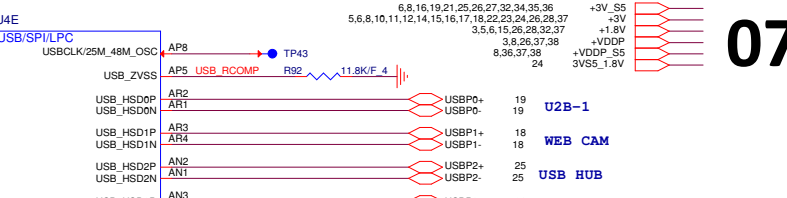
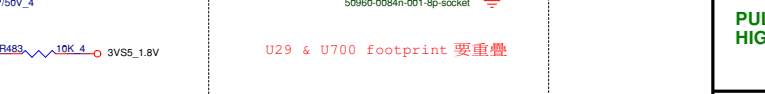
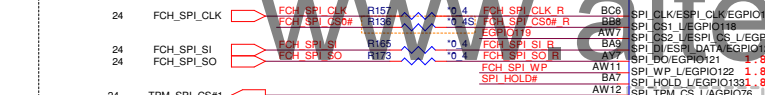
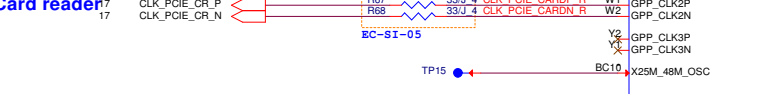
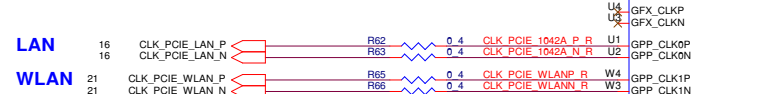
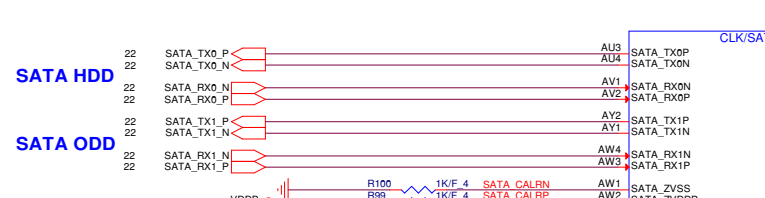
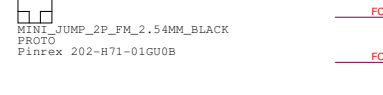
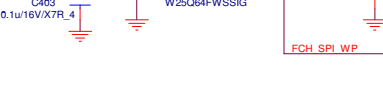
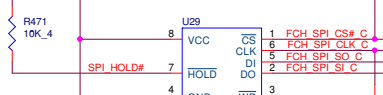
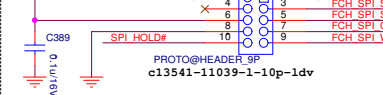
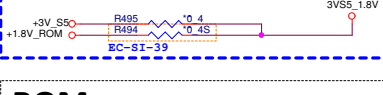
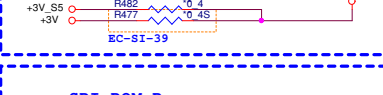
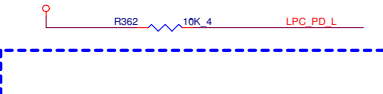
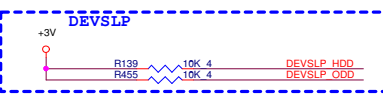
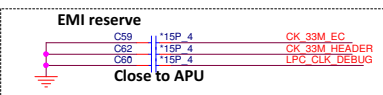
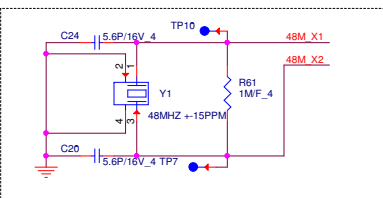
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REQUIRED STRAPS

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PULL HIGH	BOOT Fail Timer ENABLE	Internal CLKGEN ENABLE	SPI ROM	Normal Power Timing ENABLE	SPI Voltage 1.8V	Enhanced Reset logic for faster resume from S5
PULL LOW	BOOT Fail Timer DISABLE	Internal CLKGEN DISABLE	LPC ROM	Normal Power Timing DISABLE	SPI Voltage 3.3V	Traditional Reset logic

CK_33M_EC	LPC_CLK_DEBUG	LFRAME#	RTC_CLK	GEVENT2#	SYS_RST#
BOOT Fail Timer ENABLE	Internal CLKGEN ENABLE	SPI ROM	Normal Power Timing ENABLE	SPI Voltage 1.8V	Enhanced Reset logic for faster resume from S5
BOOT Fail Timer DISABLE	Internal CLKGEN DISABLE	LPC ROM	Normal Power Timing DISABLE	SPI Voltage 3.3V	Traditional Reset logic

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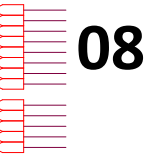
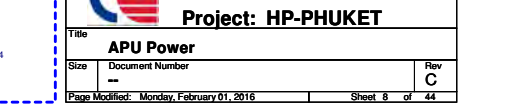
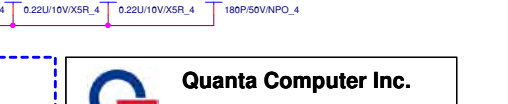
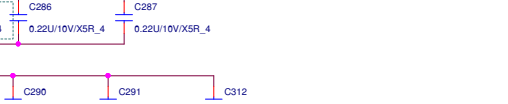
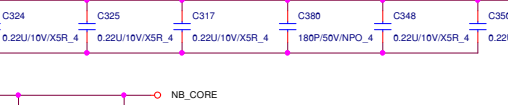
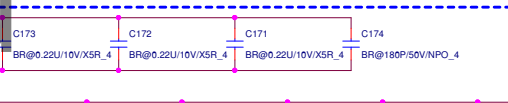
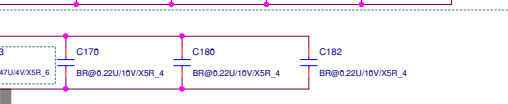
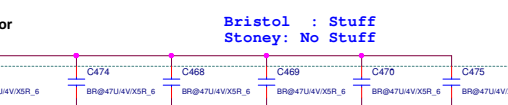
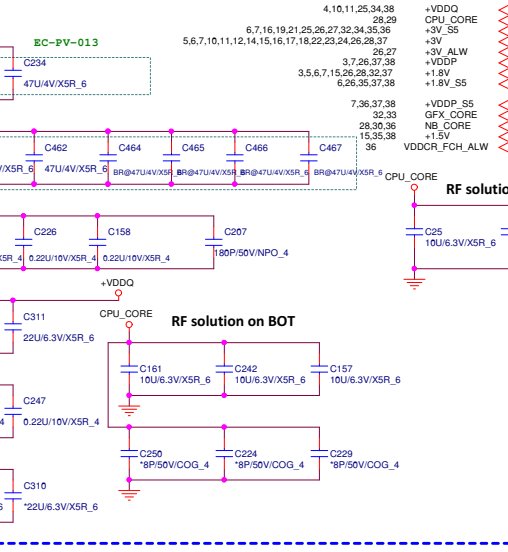
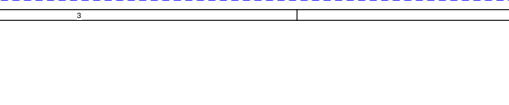
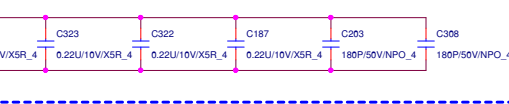
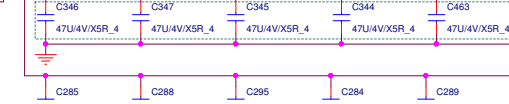
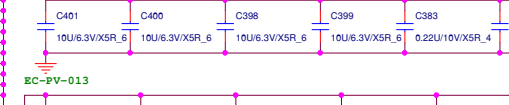
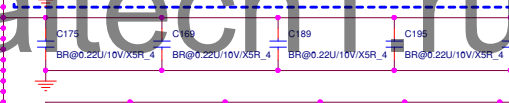
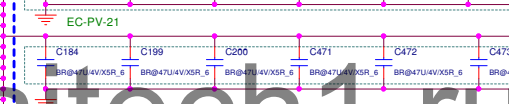
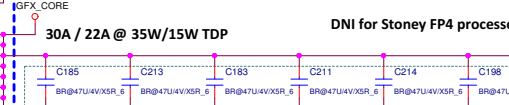
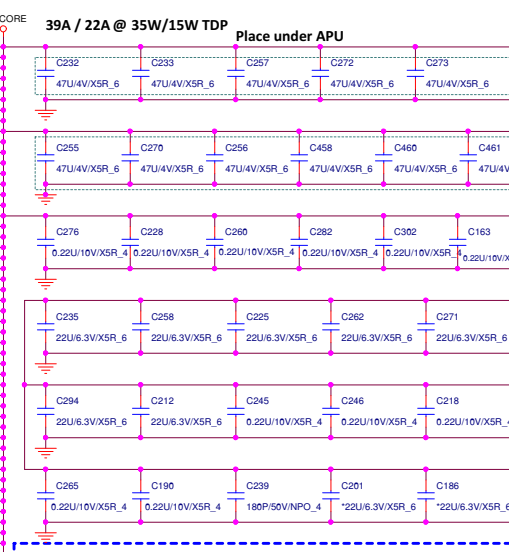
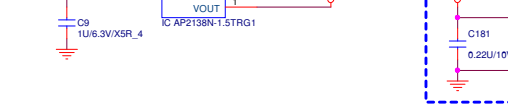
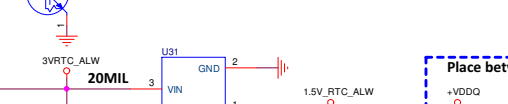
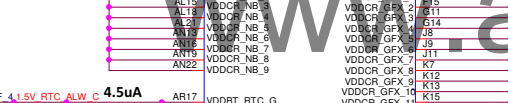
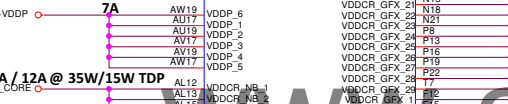
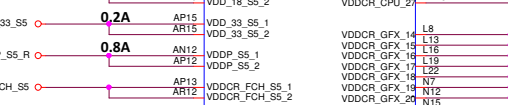
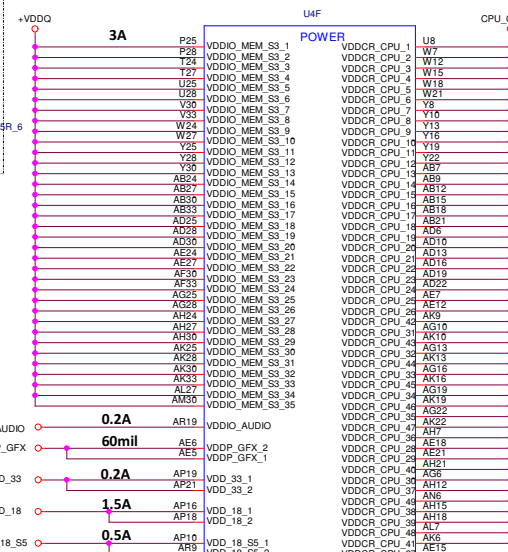
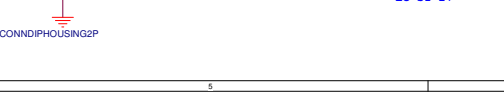
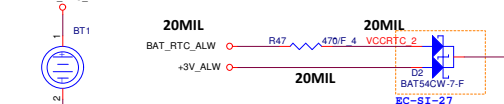
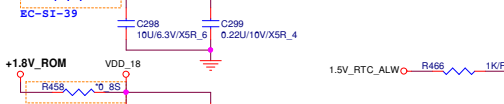
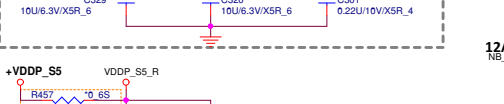
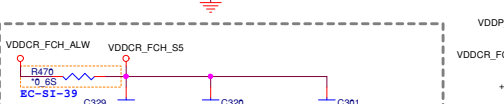
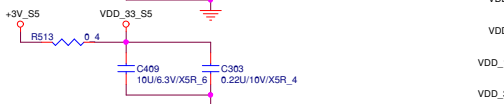
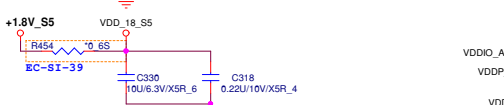
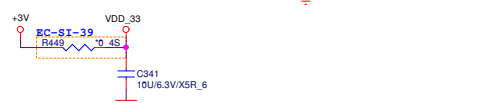
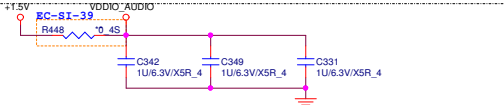
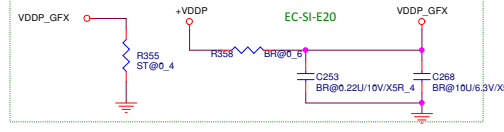
Title: CLK/USB/SATA/SPI/LPC


Size: Document Number

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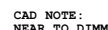
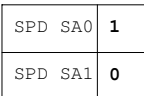
**If P_GFX [7:0] are not used,
VDDP_GFX power balls can be connected to VSS.**



	Quanta Computer Inc.	
	Project: HP-PHUKET	
Title APU Power		
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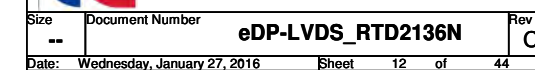
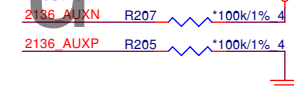






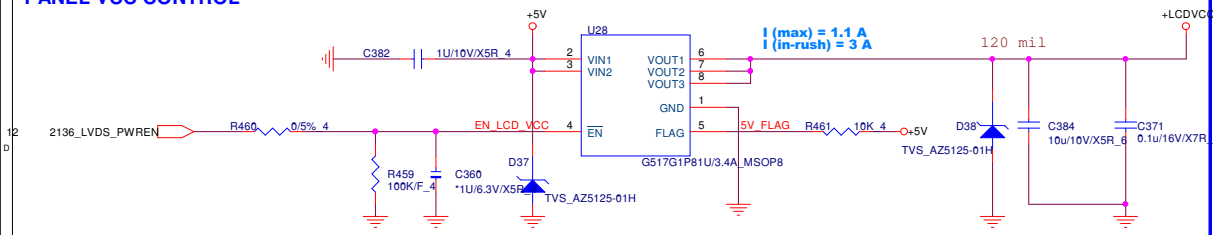
Close to pin25!

12

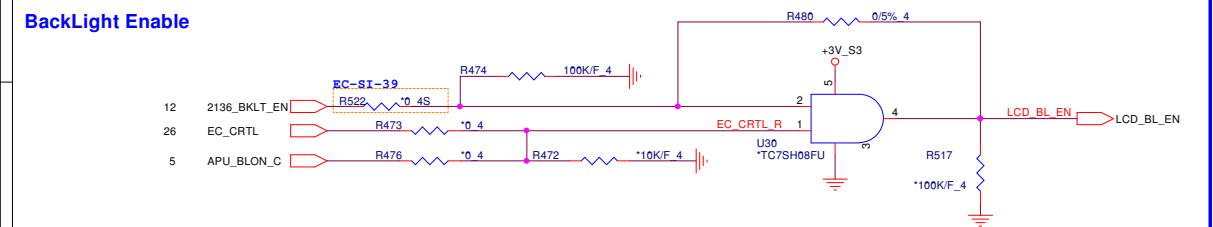


LED PANEL

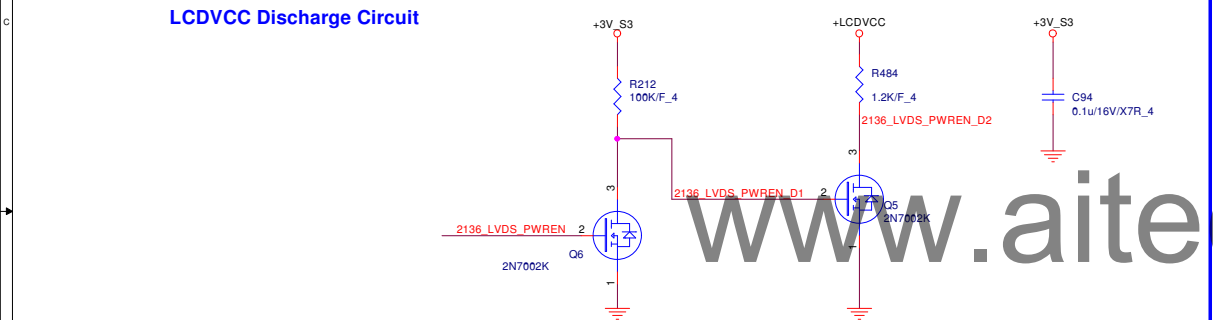
PANEL VCC CONTROL



BackLight Enable



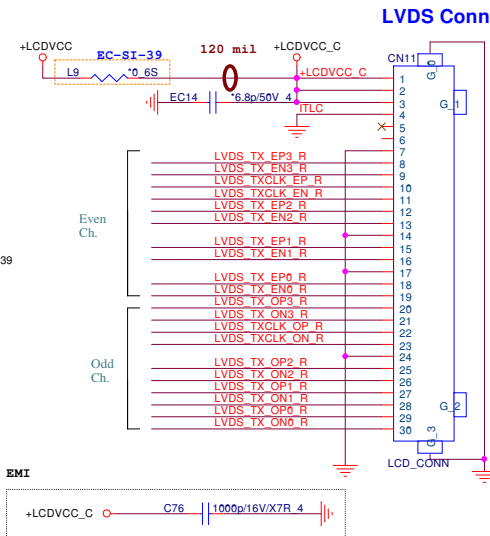
LCDVCC Discharge Circuit



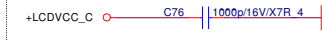
18,25,27,29,30,31,33,34,35,36,38,39
25,26,37
14,15,18,23,25,31,37,38

+VIN
+3V_S3
+5V

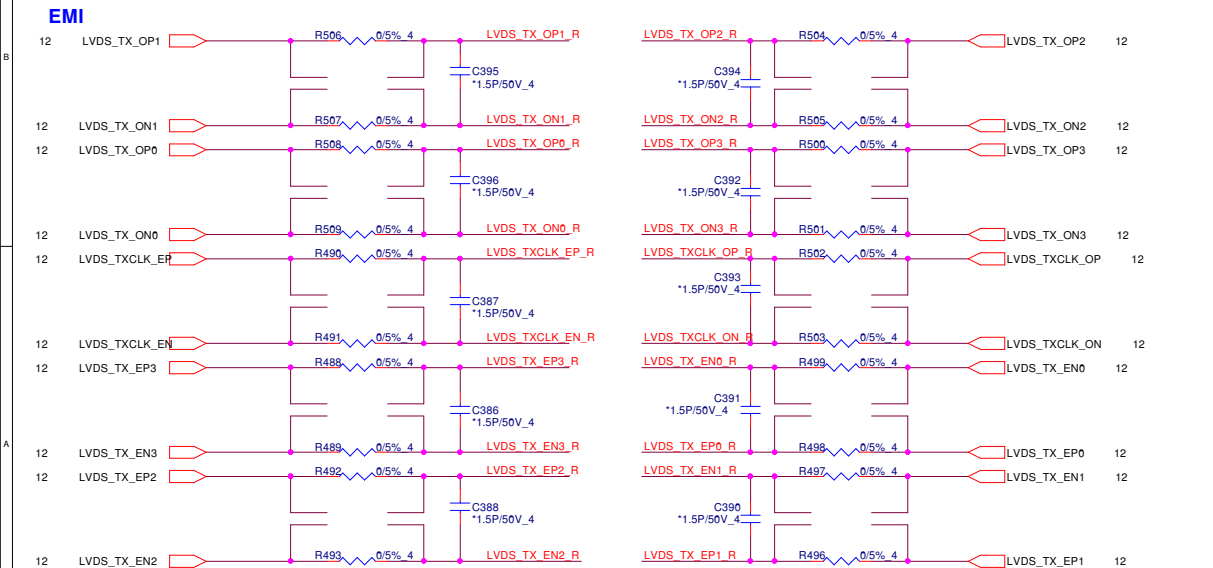
13



EMI



EMI



Quanta Computer Inc.

PROJECT HP-PHUKET

Size

Document Number

Panel (Control).LCD-Conn.

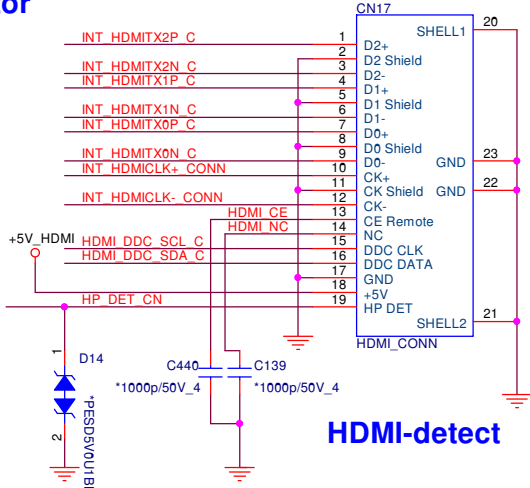
Rev

C

Date: Friday, January 29, 2016

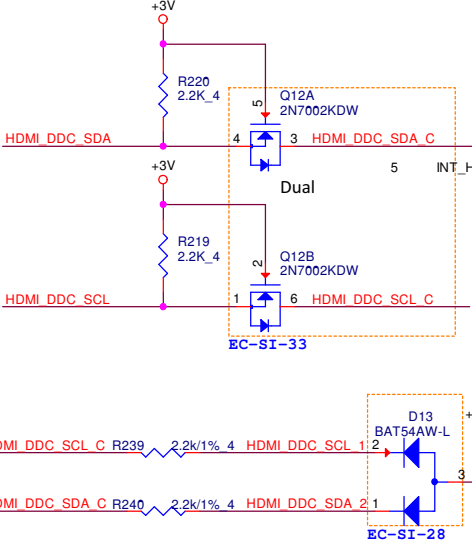
Sheet 13 of 44

HDMI connector

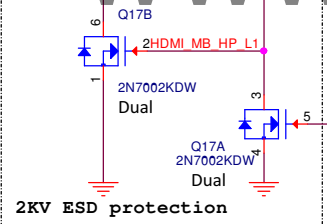


HDMI-detect

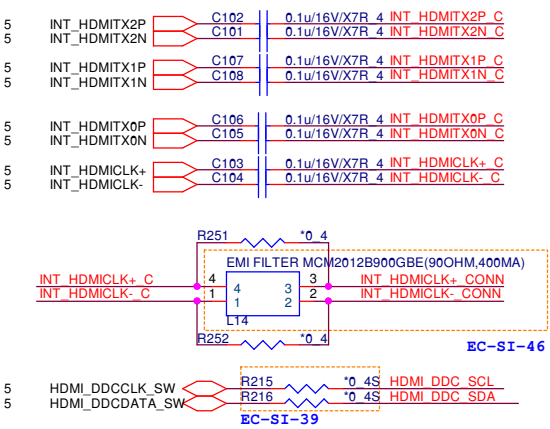
HDMI DDC



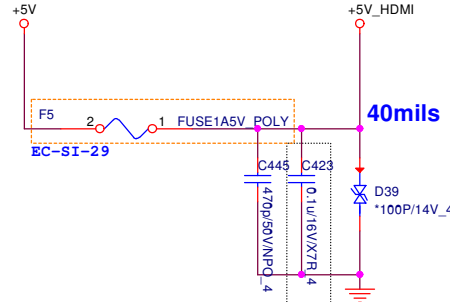
2KV ESD protection



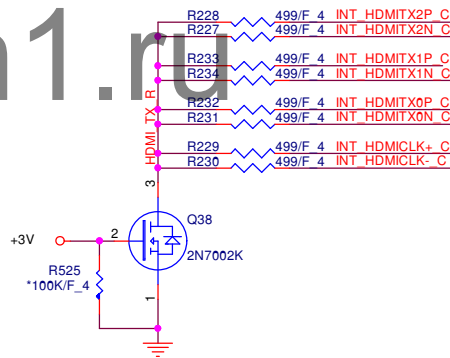
HDMI INTERFACE



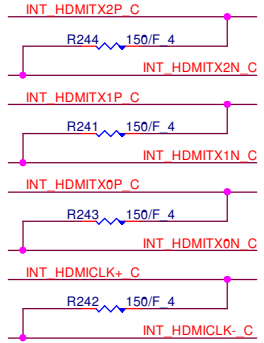
HDMI POWER SUPPLY



HDMI LEVEL SHIFT

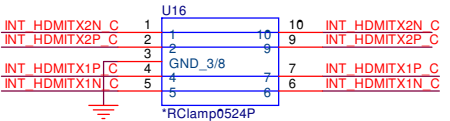
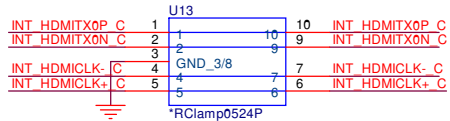
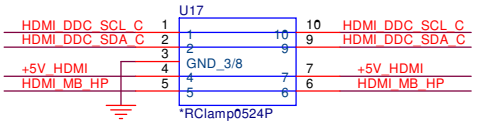



HDMI EMI (EMC)



ESD reserve for HDMI

Layout Notes:
Place decoupling CAPs close to Connector

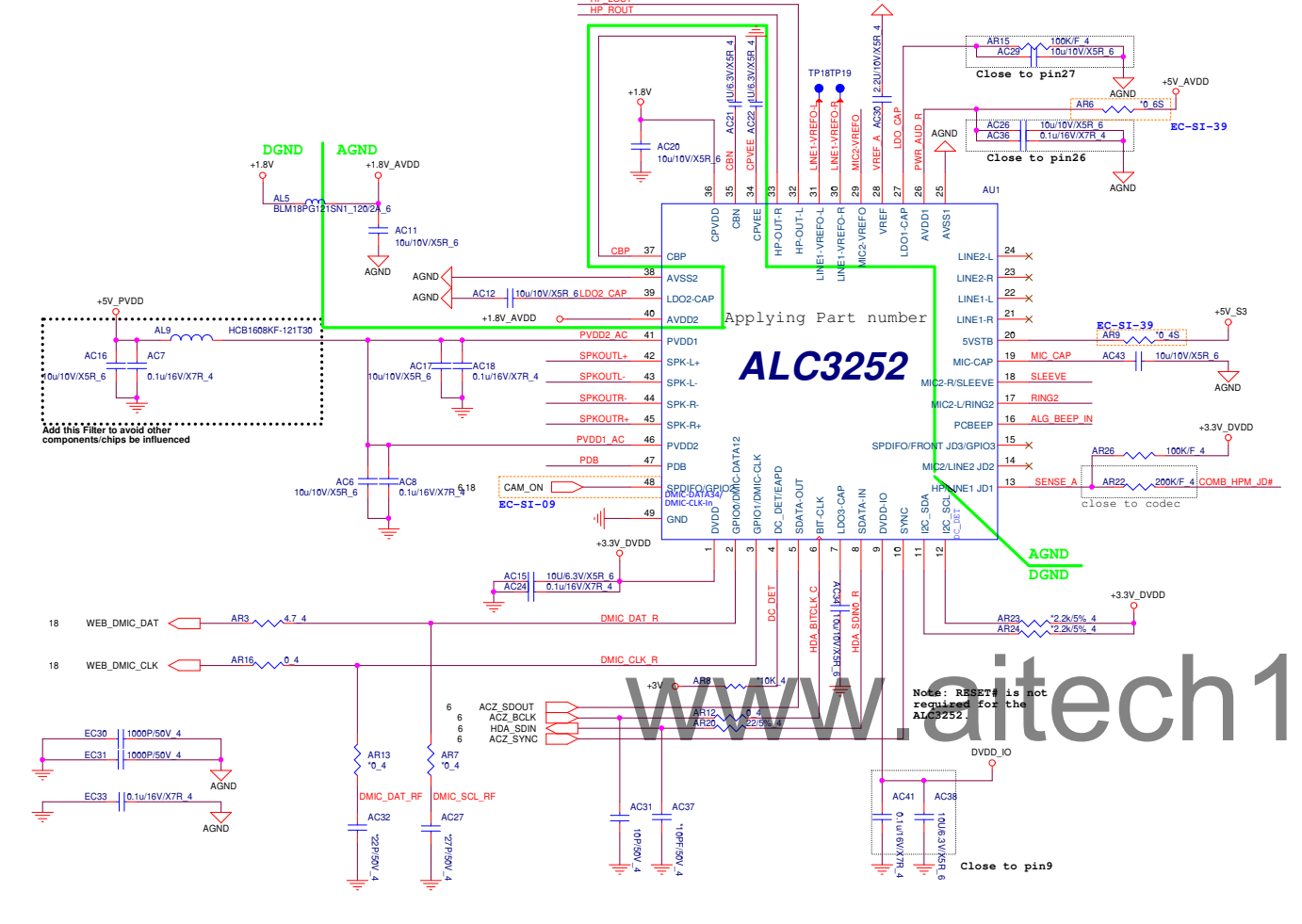




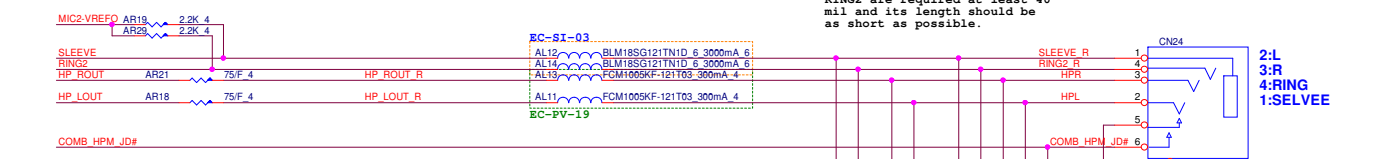
Quanta Computer Inc.
PROJECT HP-PHUKET

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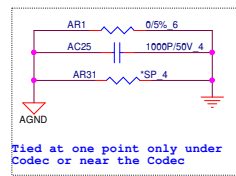
Audio Codec ALC3252



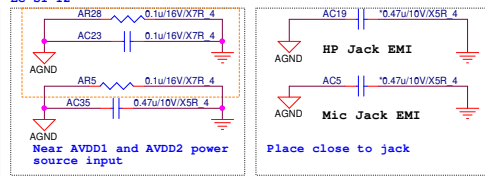
HeadPhone/Mic Combo Conn



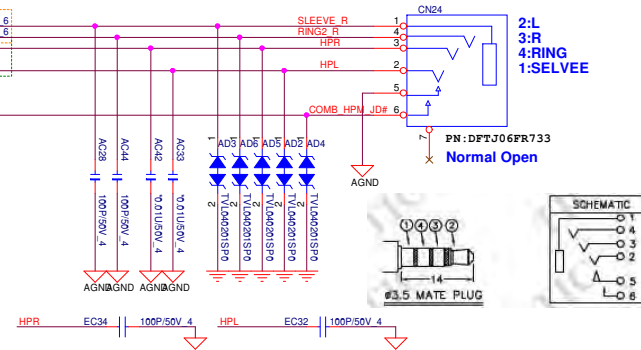
CODEC Return Path



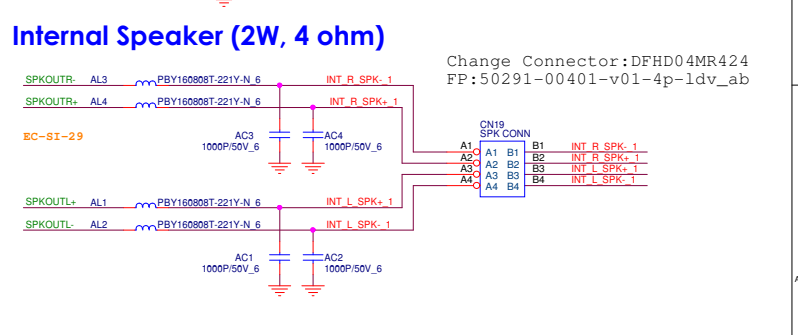
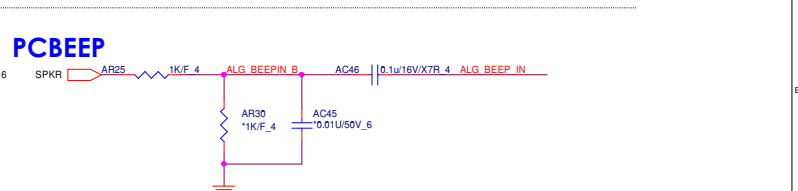
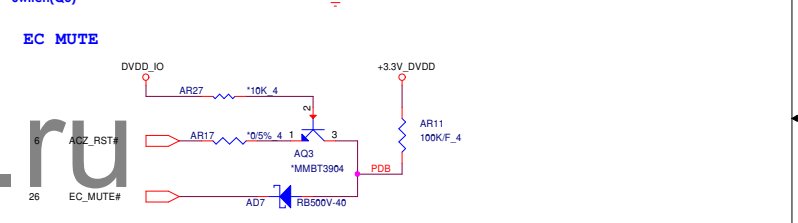
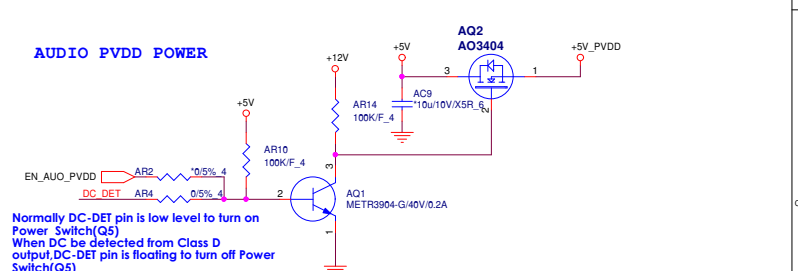
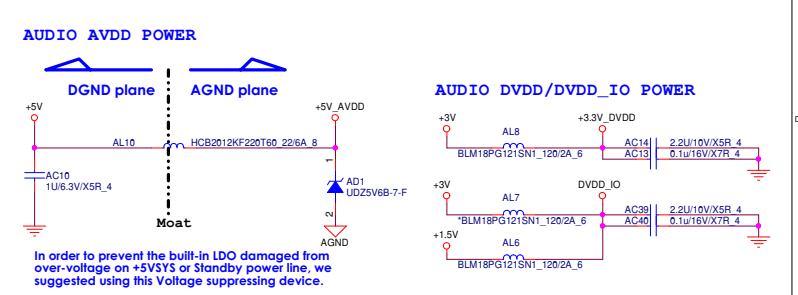
EMI



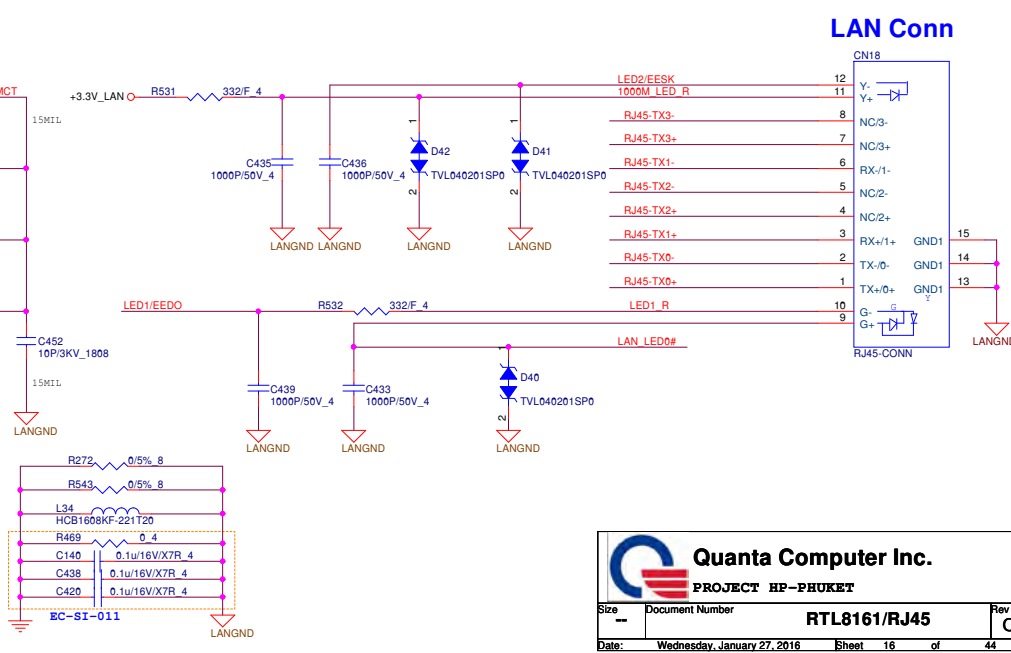
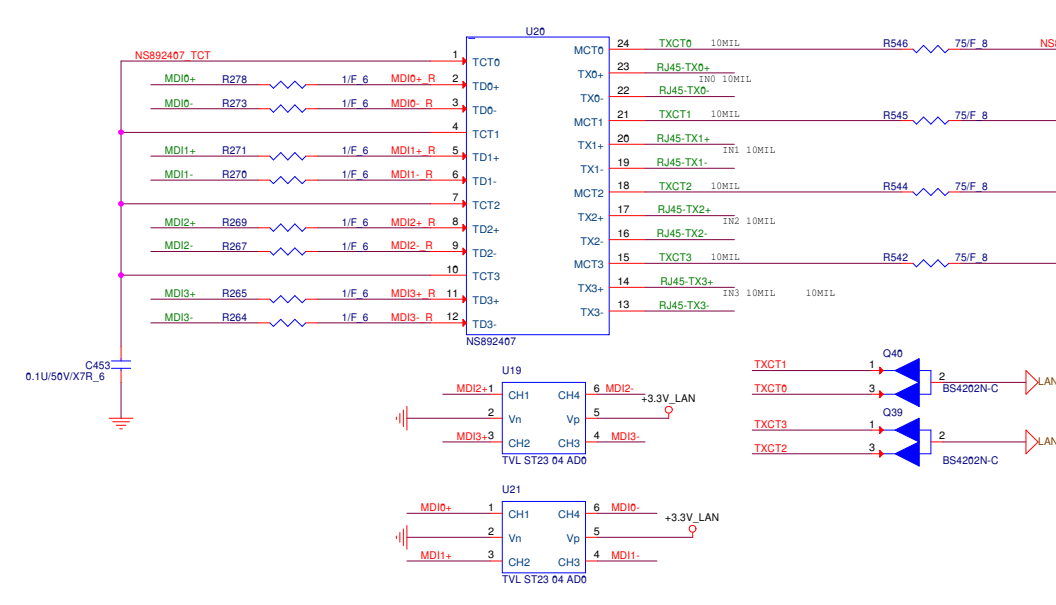
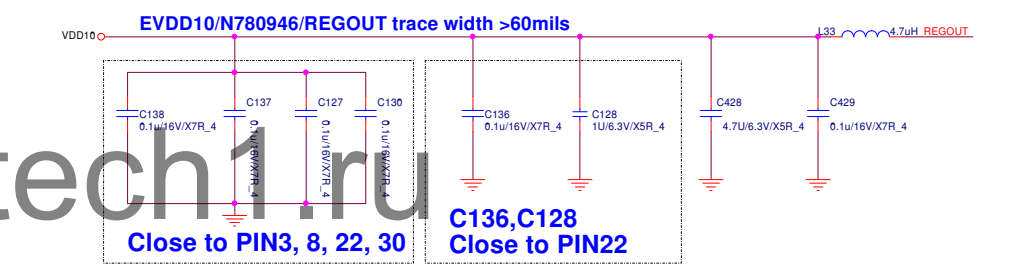
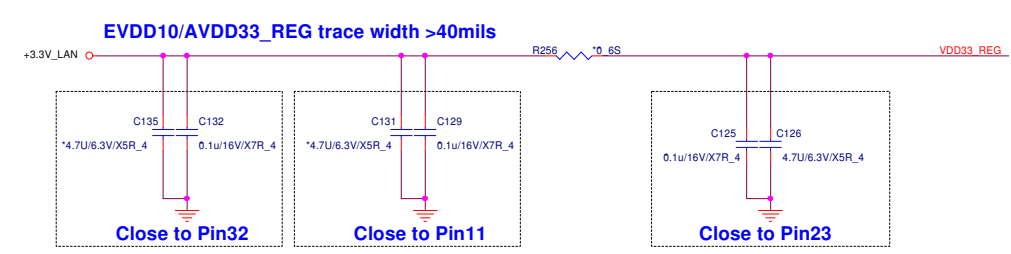
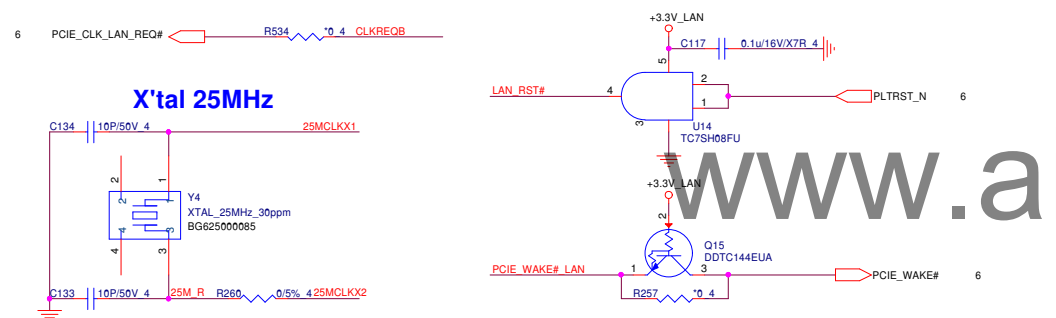
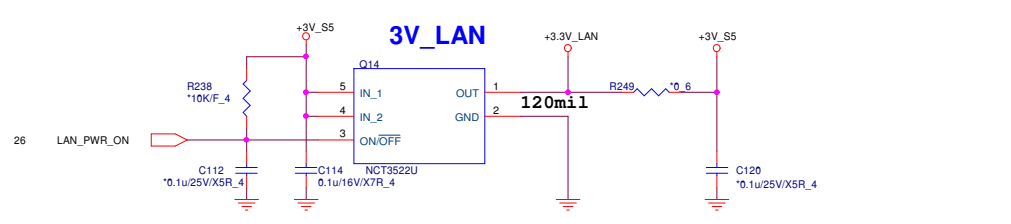
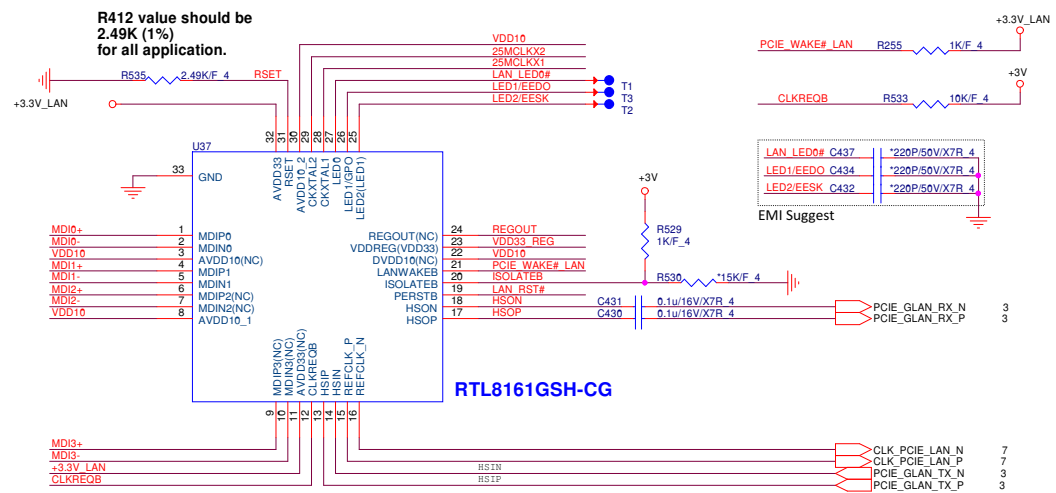
PCB trace width of SLEEVE & RING2 are required at least 40 mil and its length should be as short as possible.




15



LAN (RTL8161GSH) 10/100/1000

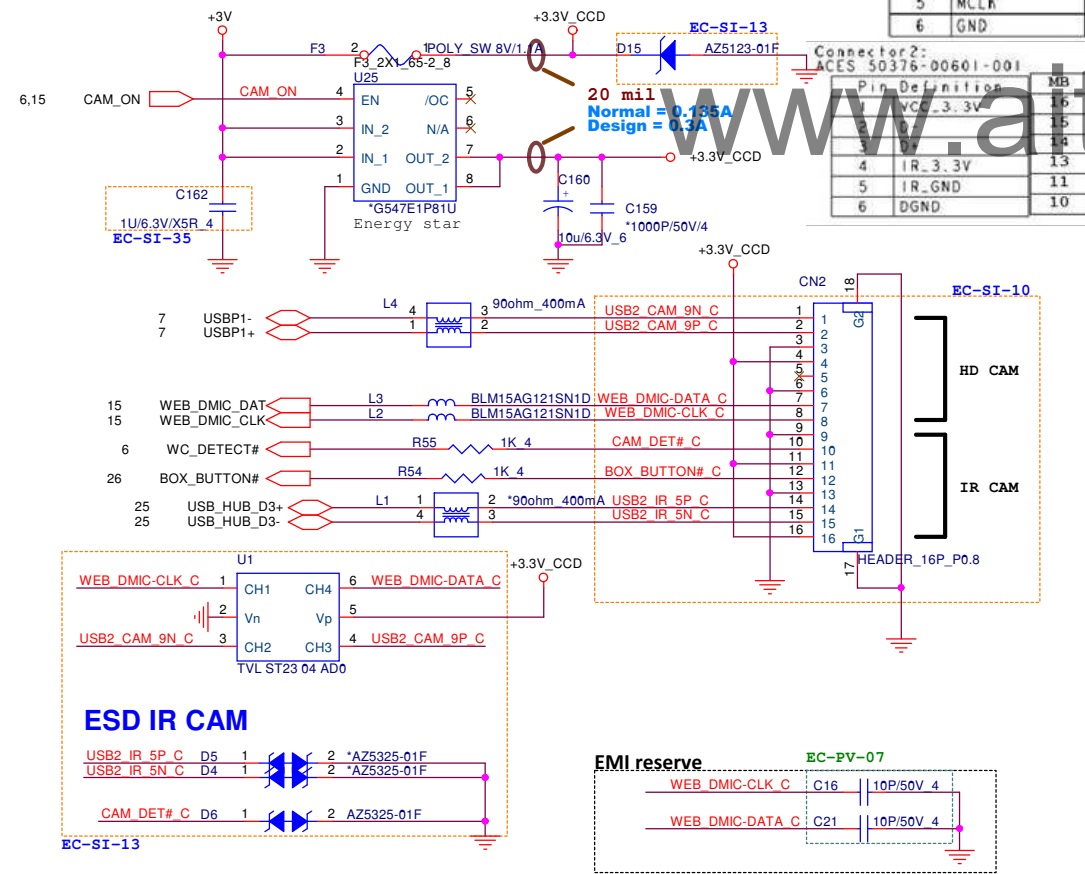




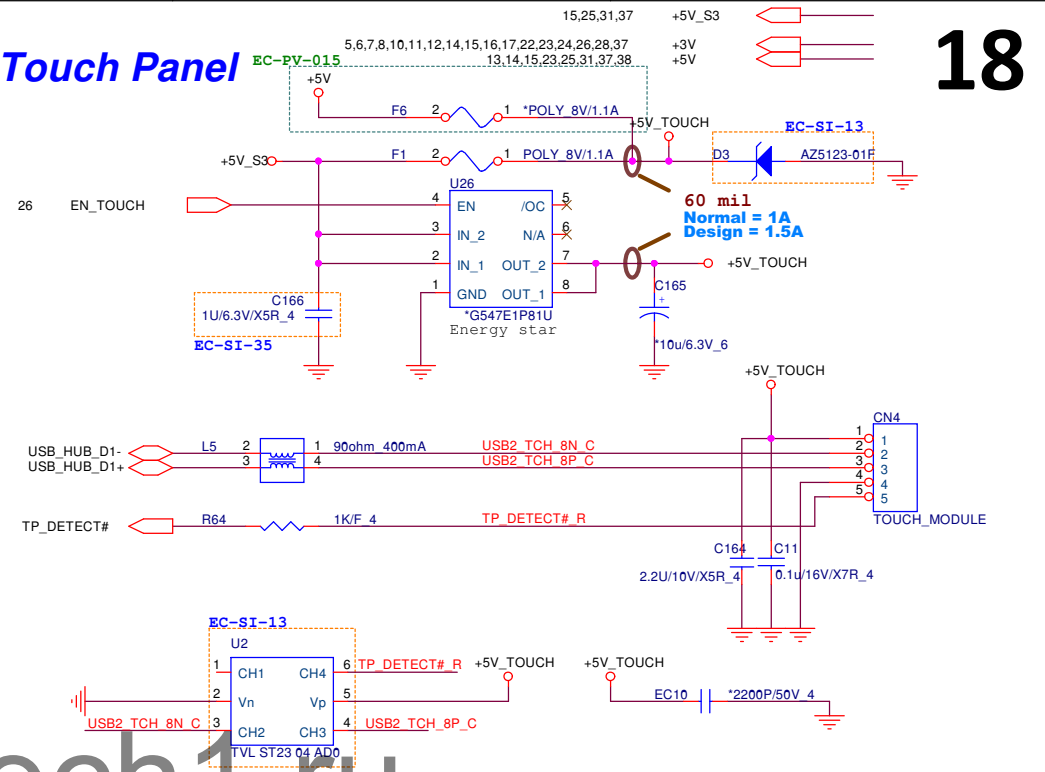
 Quanta Computer Inc. PROJECT HP-PHUKET			
Size	Document Number	Card Reader (RTS5239)	Rev
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(Optional 1: 3DCAM+DMIC)

(Optional 2: WEBCAM+DMIC)



Touch Panel



DC_IN LED

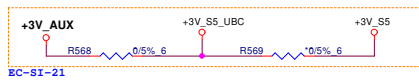
SATA LED

ESD for 3D CAM

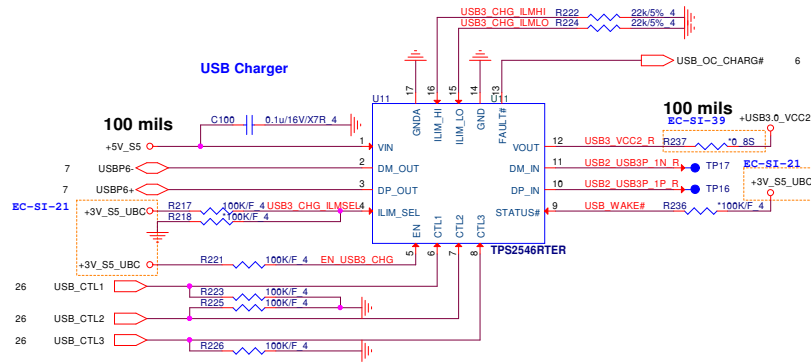
USD protection diodes for ESD.
as close as possible to USB connector pins.

USB PORT

USB3.0 Charging Port



USB Charger



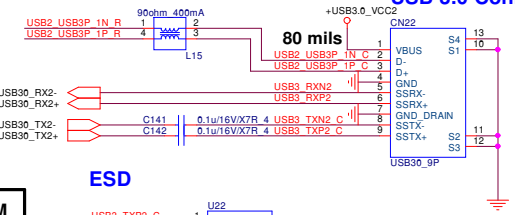
SDP : Standard Downstream Port
CDP : Charging downstream port
DCP : Dedicated Charging Port
Enable/Disable : setting by BIOS

POWER STATE	TPS2546 CHARGING MODE	CTRL1	CTRL2	CTRL3	ILIM
S0	CDP LOAD DETECTION WITH ILIM_LO +60mA THRESHOLDS OR IF A BC1.2 PRIMARY DETECTION OCCURS	1	1	1	1
S3	AUTO MODE, LOAD DETECTION WITH POWER WAKE THRESHOLD	0	1	1	1
S4/S5	AUTO MODE, KEYBOARD/ MOUSE WAKE-UP, LOAD DETECTION WITH ILIM_LO +60mA THRESHOLDS	0	0	1	1

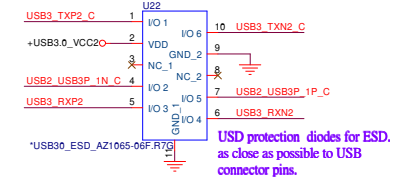
6,7,8,16,21,25,26,27,32,34,35,36
15,25,31,37
23,25,27,28,32,34,35,36,37

+3V_S5
+5V_S3
+5V_S5

USB 3.0 Conn.

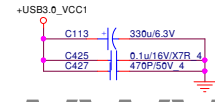
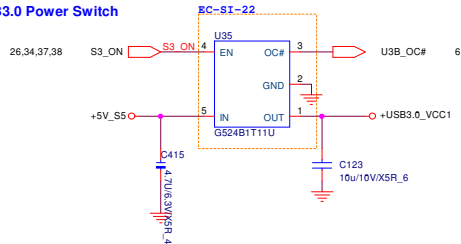


ESD

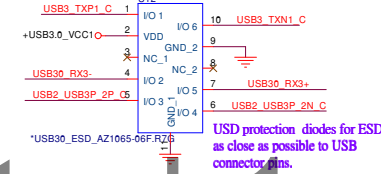


USB3.0 PORT

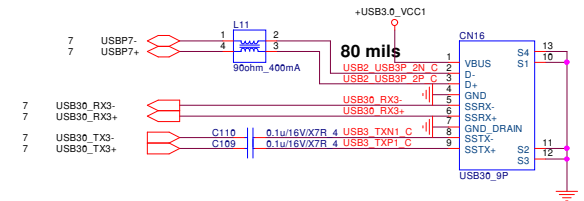
USB3.0 Power Switch



ESD

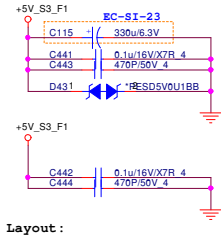
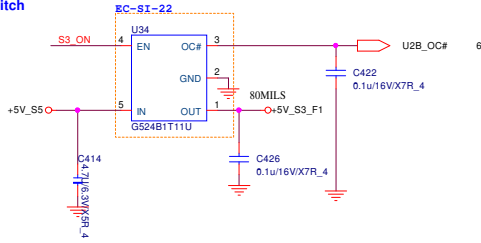


USB3.0 Conn



USB2.0 X 2

USB3.0 Power Switch



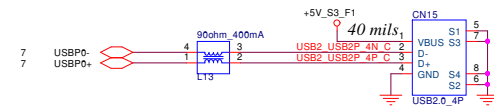
Layout :
1. All caps Near to Connector
2. Place D43 near CN21 and CN22

ESD

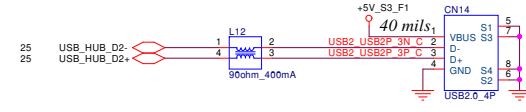


USB2.0 Conn

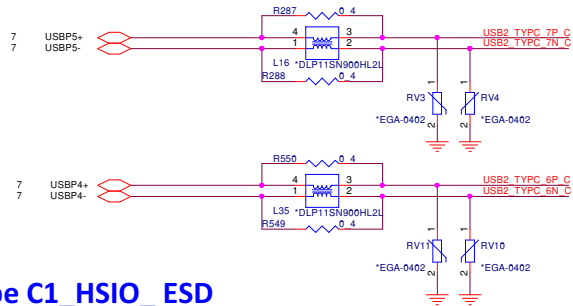
USB2_Port0



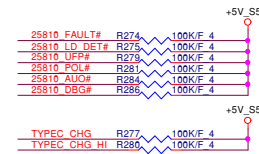
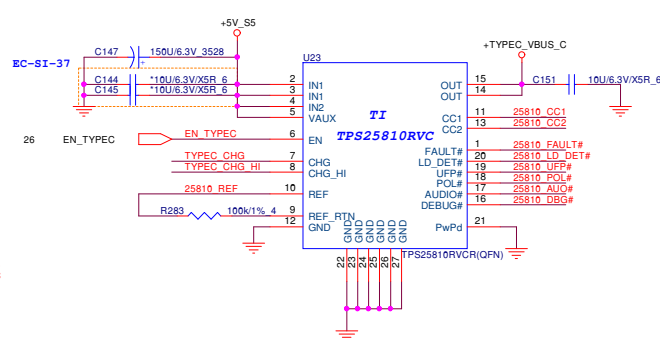
USB2_HUB_Port2



USB2.0 ESD

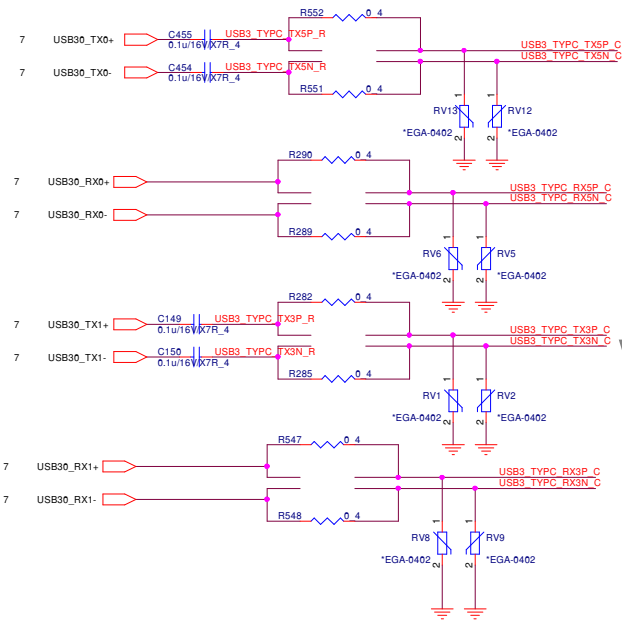


Vendor suggest input cap 120u



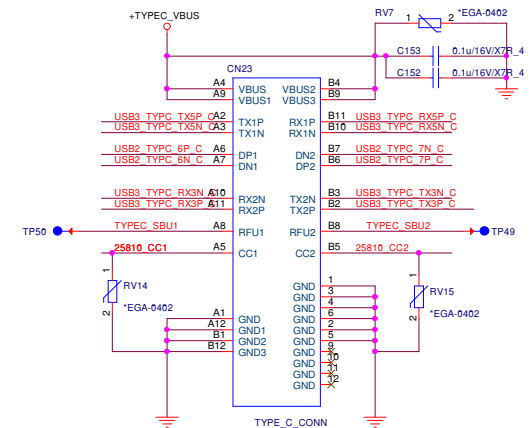
CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

Type C1_HSIO_ESD



www.aitech1.ru

TPS25810 Port	CC1	CC2	OUT	VCONN On CC1 or CC2	TPS25810 Response POLb	UFPb	AUDIOb	DEBUGb
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	LOW	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	Ra	UPE-N	UPE-N	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug Accessory Connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	LOW
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z



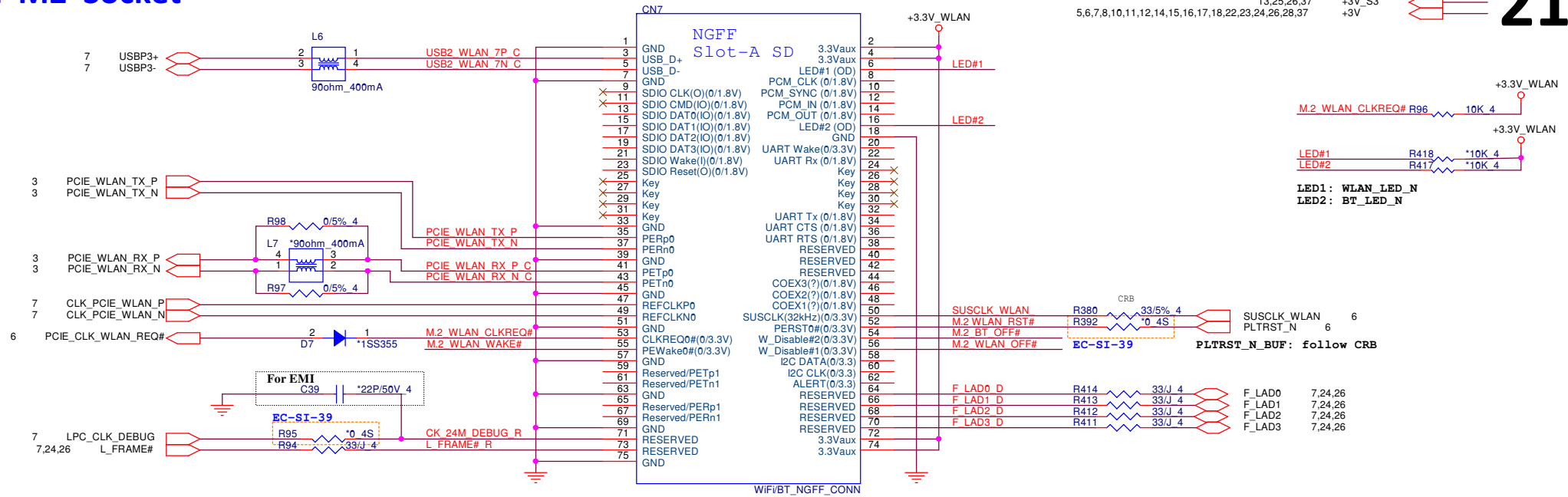
NGFF M2 Socket

H=9.0

13,25,26,37
5,6,7,8,10,11,12,14,15,16,17,18,22,23,24,26,28,37

+3V_S3
+3V

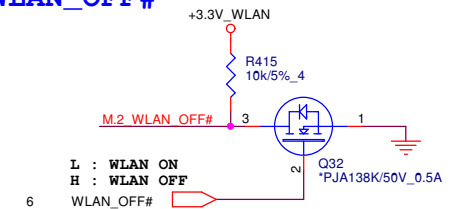
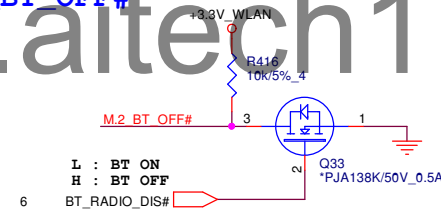
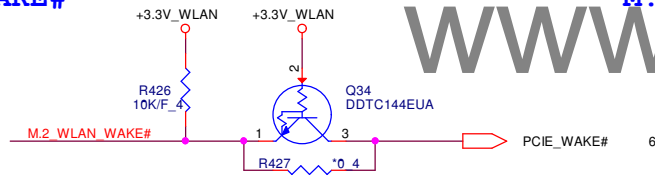
21



M.2 WLAN WAKE#

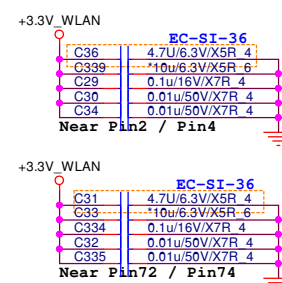
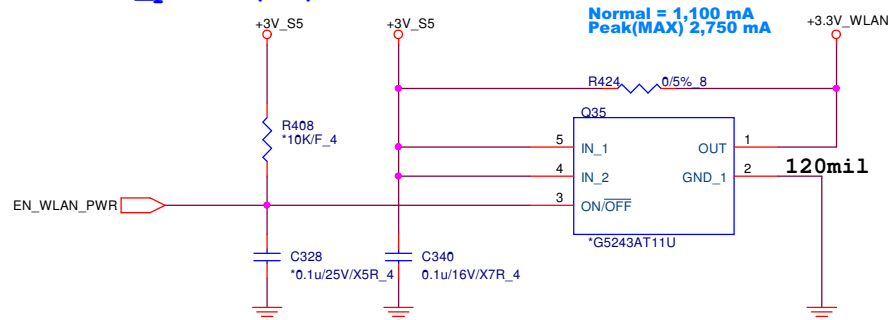
M.2 BT OFF#

M.2 WLAN_OFF#



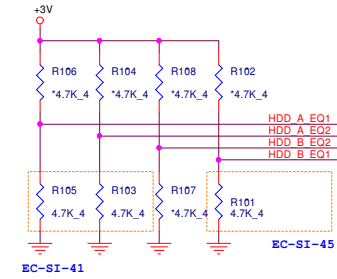
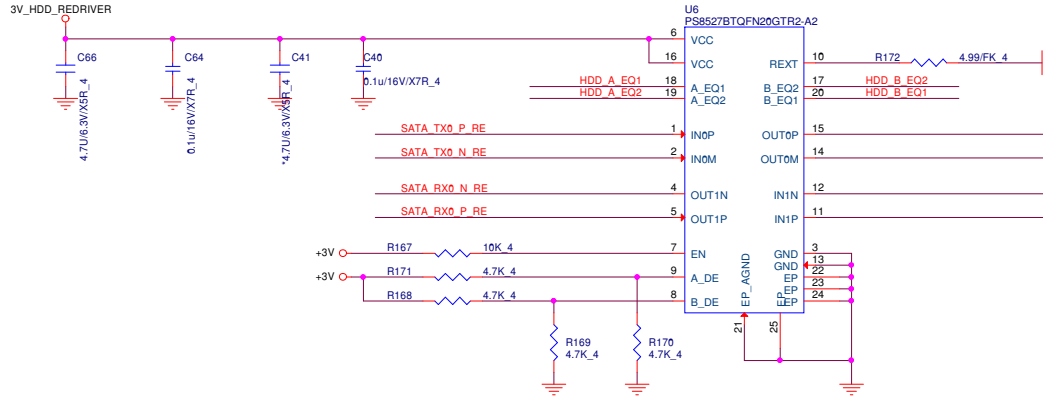
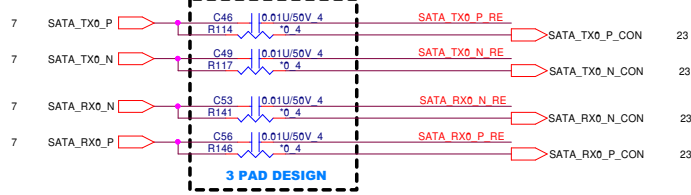
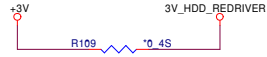
NGFF M2_power (S5)

Normal = 1,100 mA
Peak(MAX) 2,750 mA



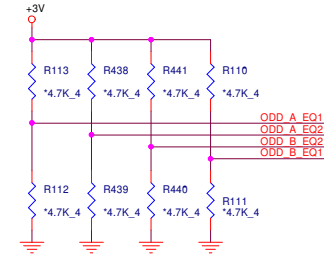
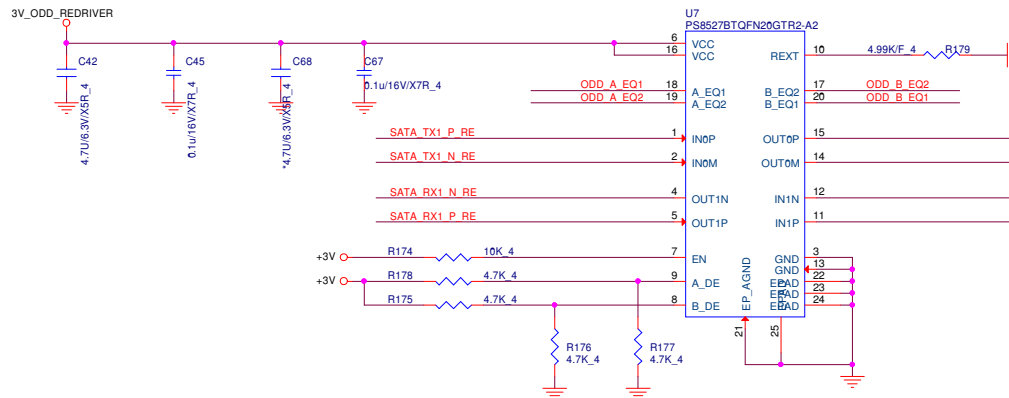
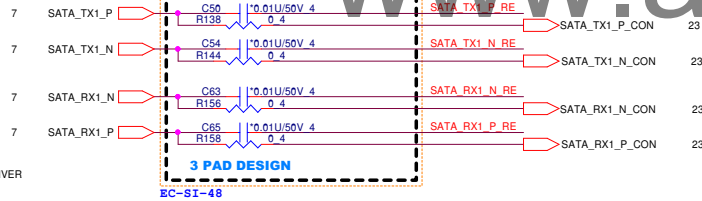
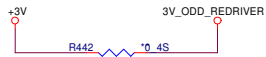
HDD REDRIVER

C46,C49,C53,C56 CLOSE TO RE-DRIVER IC



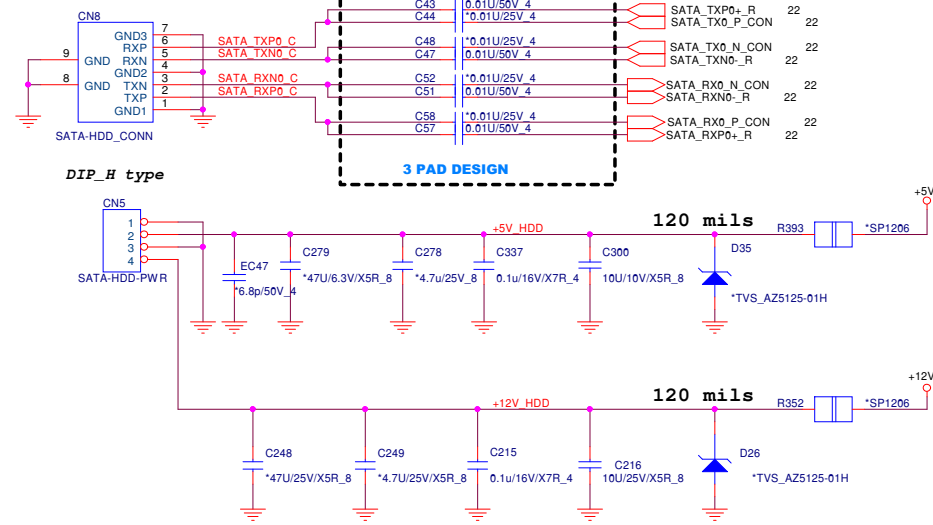
ODD REDRIVER

C50,C54,C63,C65 CLOSE TO RE-DRIVER IC



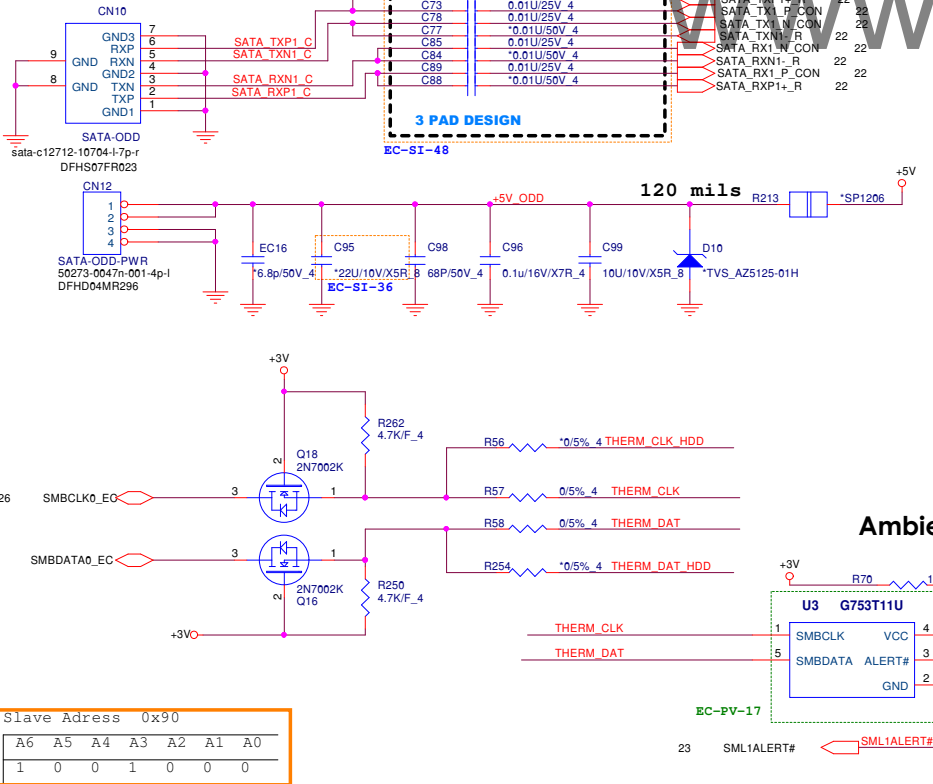
SATA HDD

HDD SATA Conn.

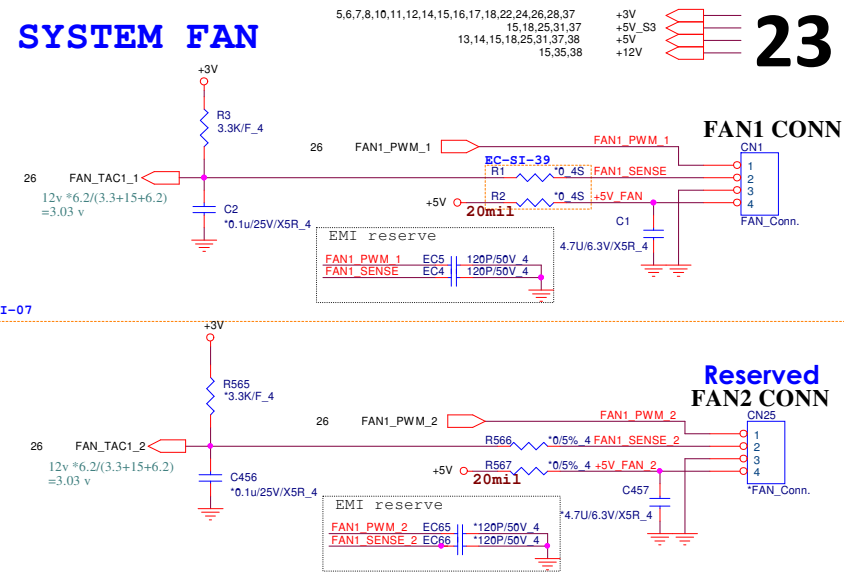


SATA ODD

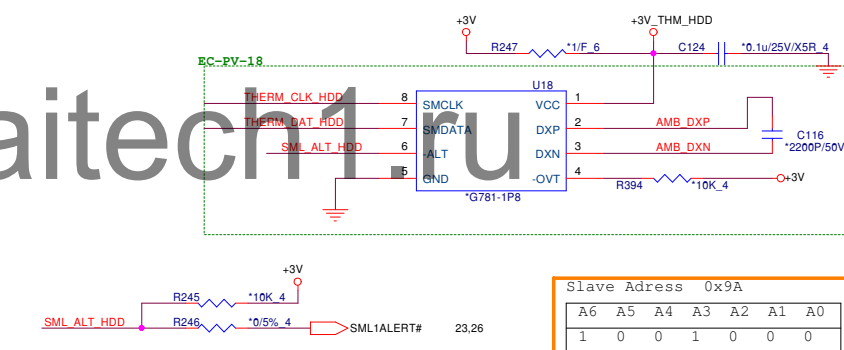
ODD SATA Conn.



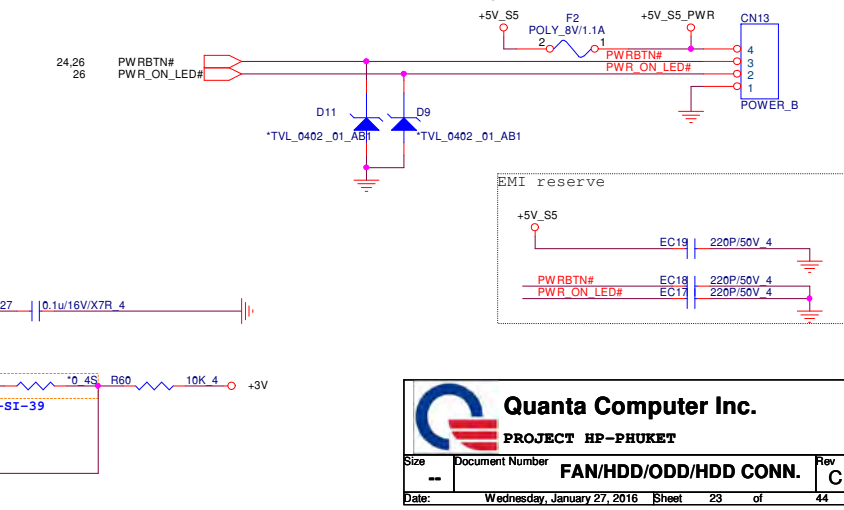
SYSTEM FAN

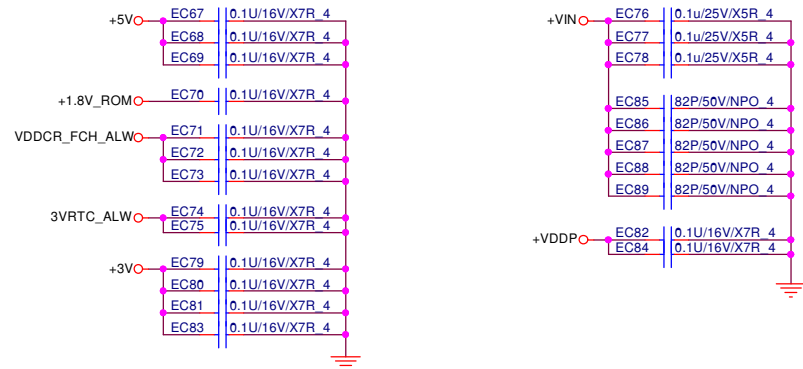


Ambient THERMAL SENSOR-HDDReserved

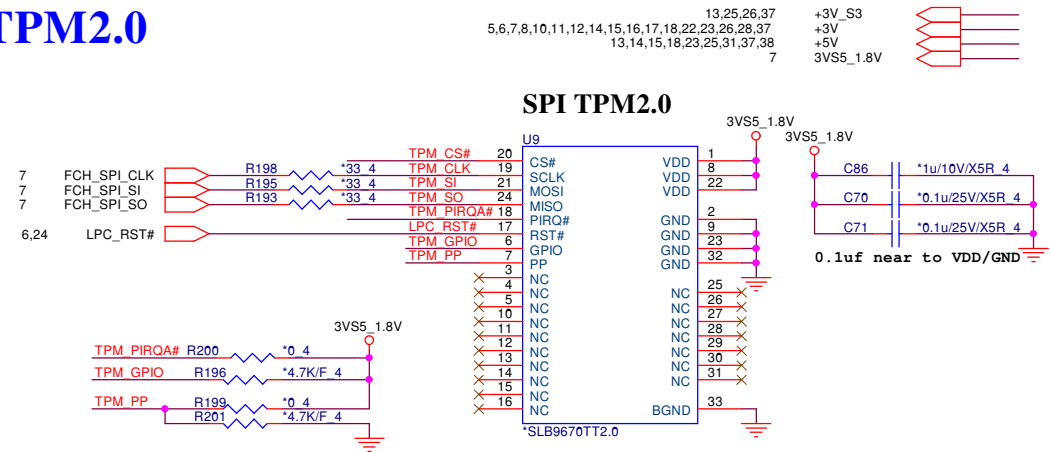


Power Button.

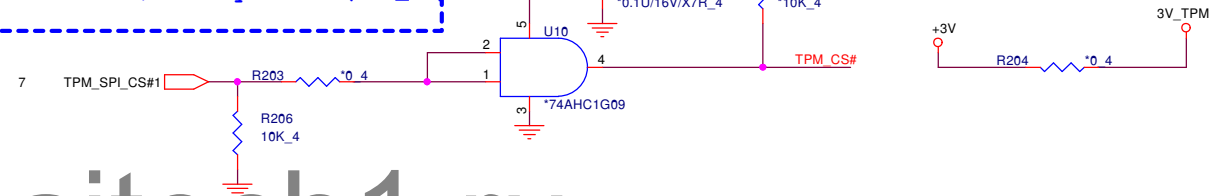




TPM2.0

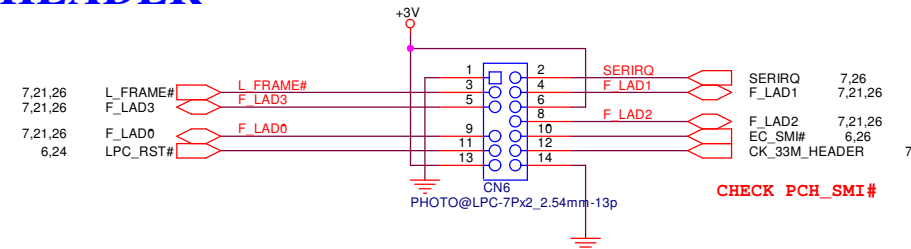


SPI TPM2.0 --SPI CS# pin
Bristol / Stoney : 3V (VDD_33)



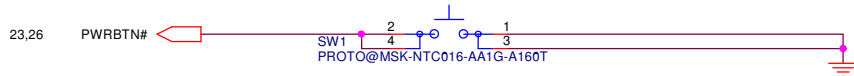
TPM_SPI_CS#1 Pull Down if no use

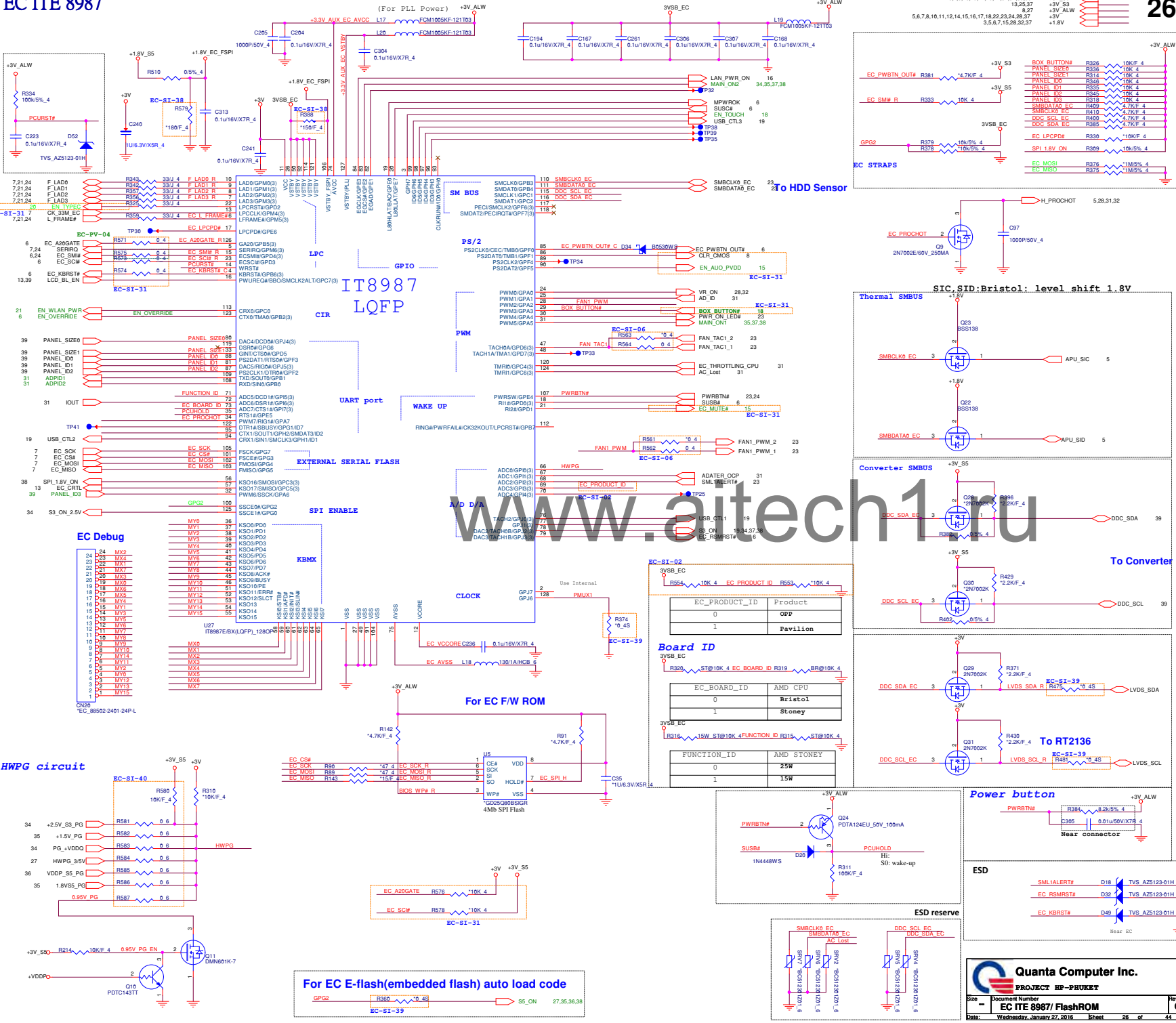
LPC HEADER

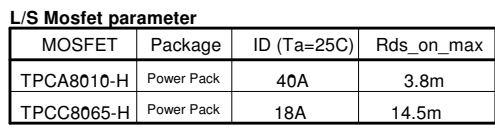


CHECK PCH_SMI#

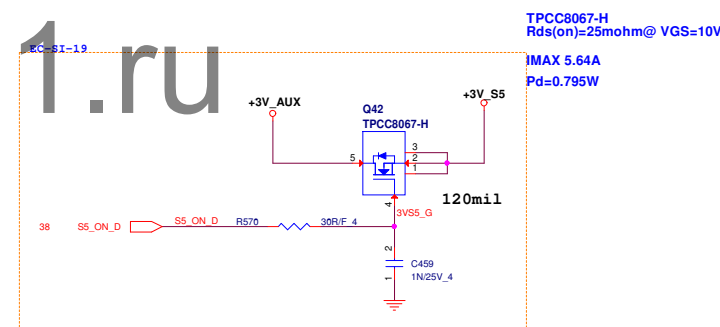
SW1 For Debug.MP will remove it.

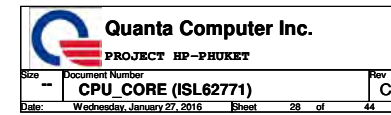






EN0	ENC	REF	VREG3	VREG5	SMPS1	SMPS2
LOW	LOW	OFF	OFF	OFF	OFF	OFF
> 2.4V	LOW	ON	ON	ON	OFF	OFF
> 2.4V	> 2.4V	ON	ON	ON	ON	ON





Bristol Ridge
CPU_CORE

TDC = 39A
EDC = 55A
OCP = 71A

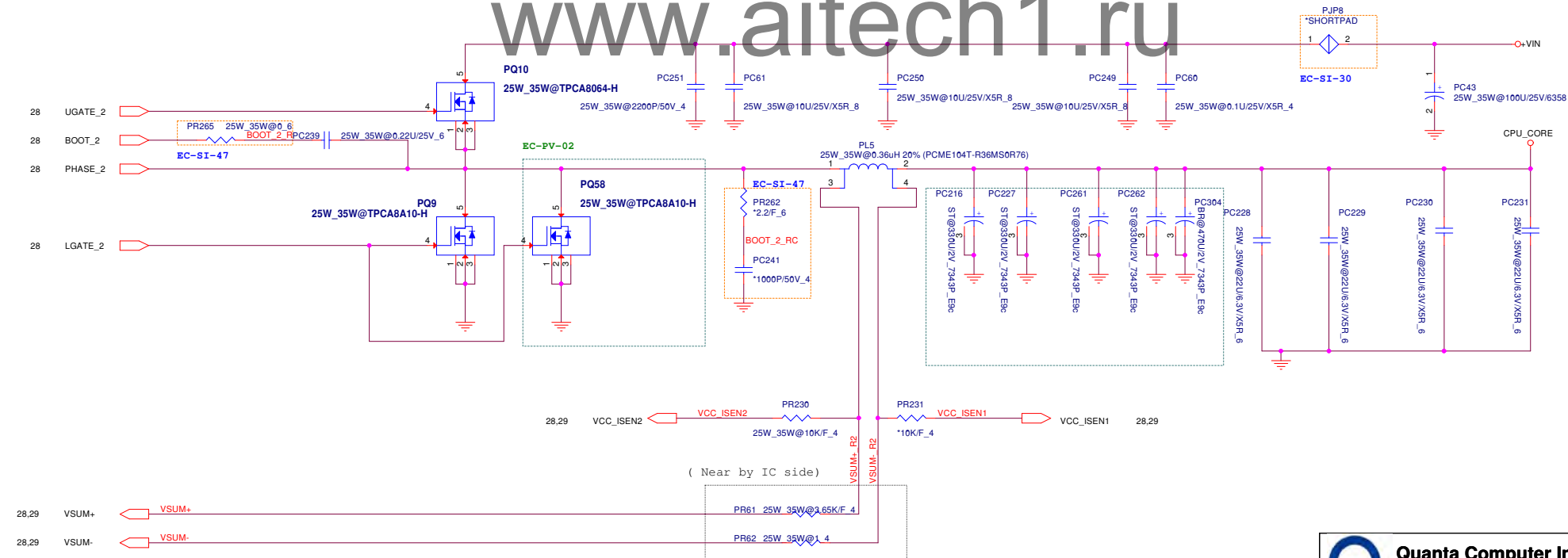
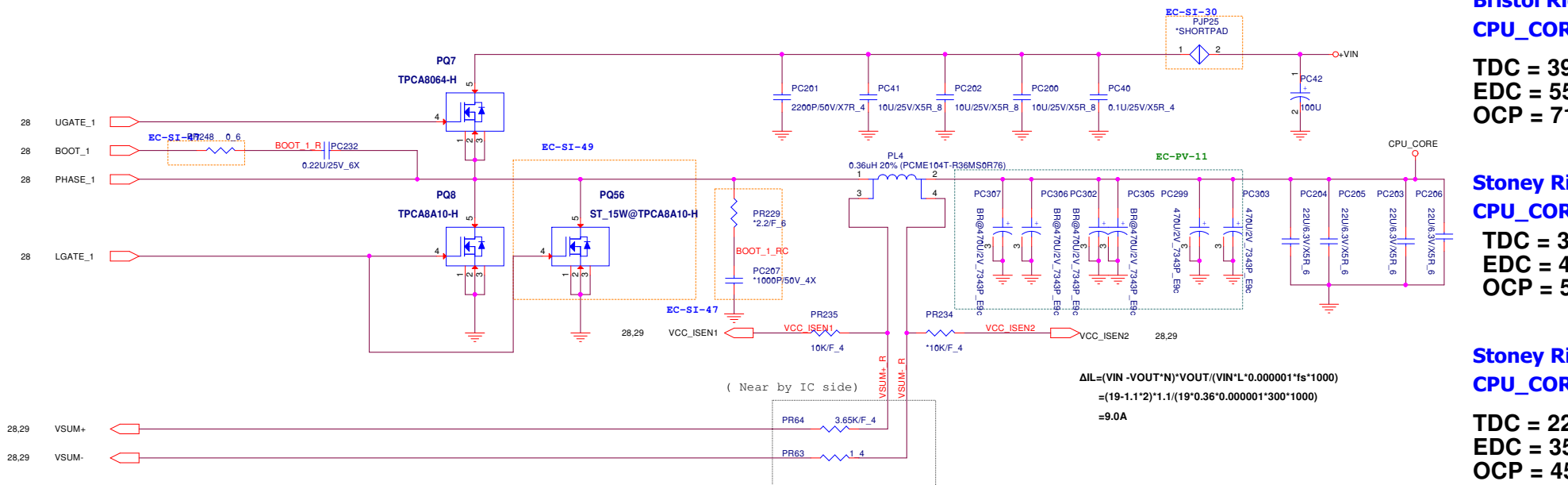
Stoney Ridge 25W
CPU_CORE

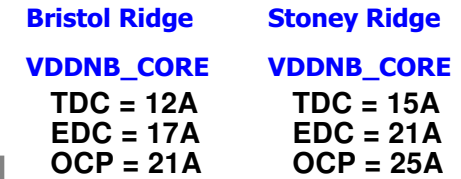
TDC = 31A
EDC = 45A
OCP = 58A

Stoney Ridge 15W
CPU_CORE

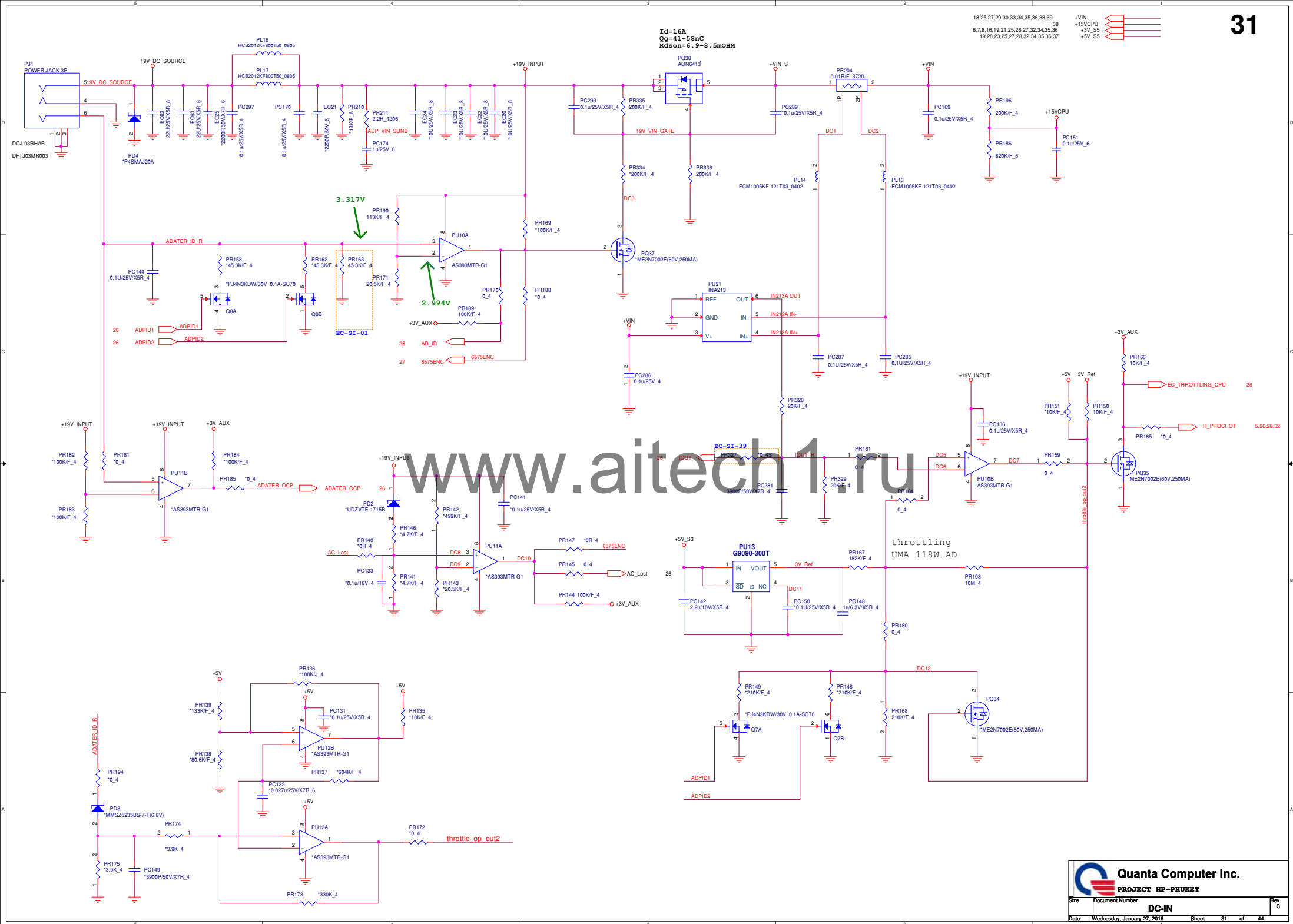
TDC = 22A
EDC = 35A
OCP = 45A

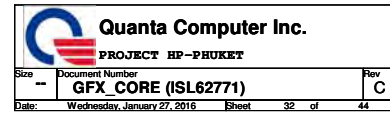
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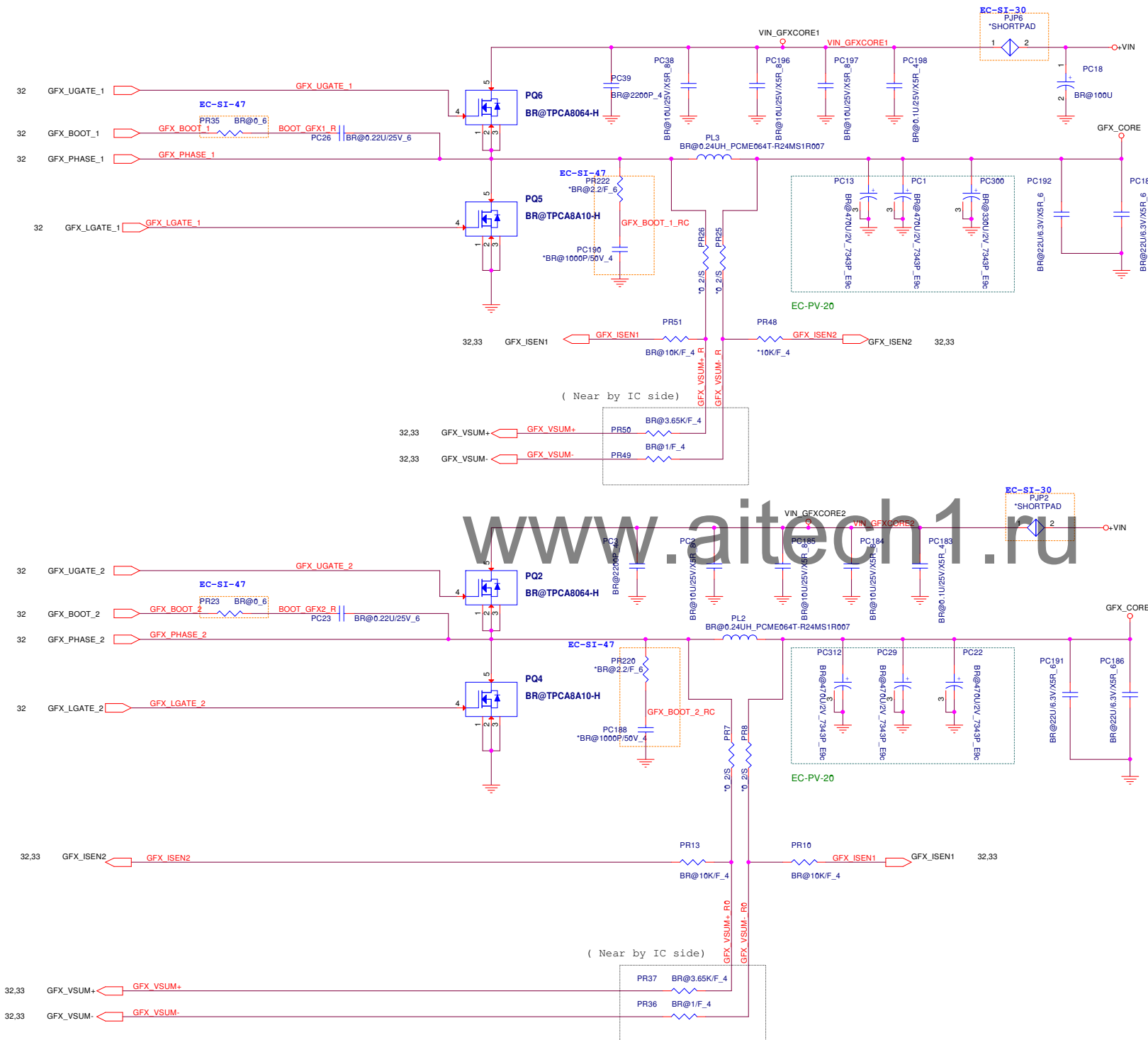
GFX_CORE

TDC = 30A
EDC = 45A
OCP= 58A

$$\Delta IL = (VIN - VOUT) * VOUT / (VIN * L * 0.000001 * fs * 1000)$$

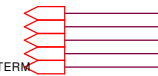
$$= (19 - 1.1) * 2 * 1.1 / (19 * 0.24 * 0.000001 * 300 * 1000)$$

$$= 13.5A$$

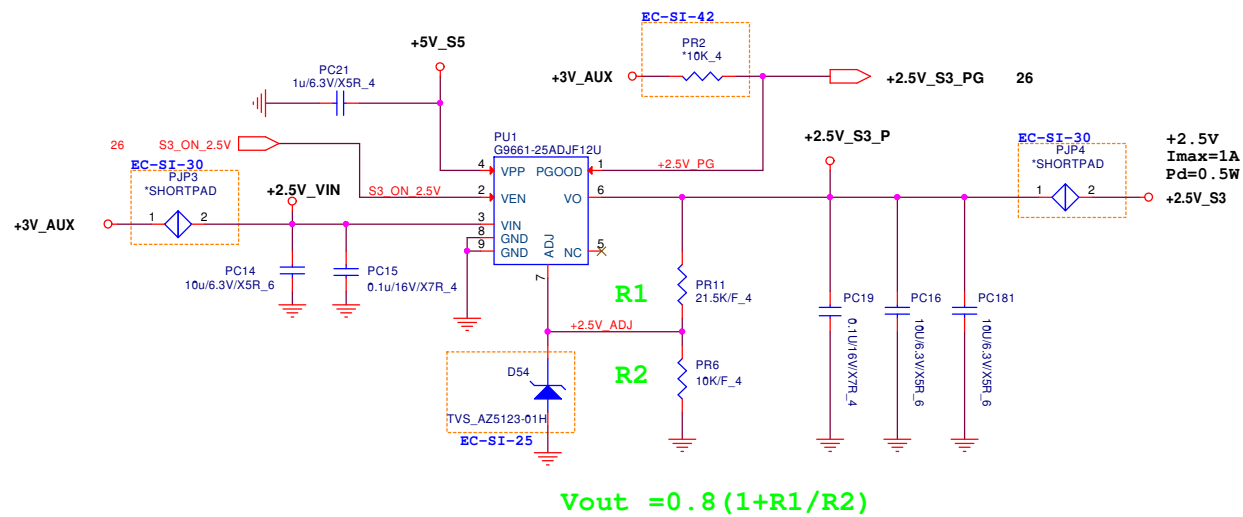
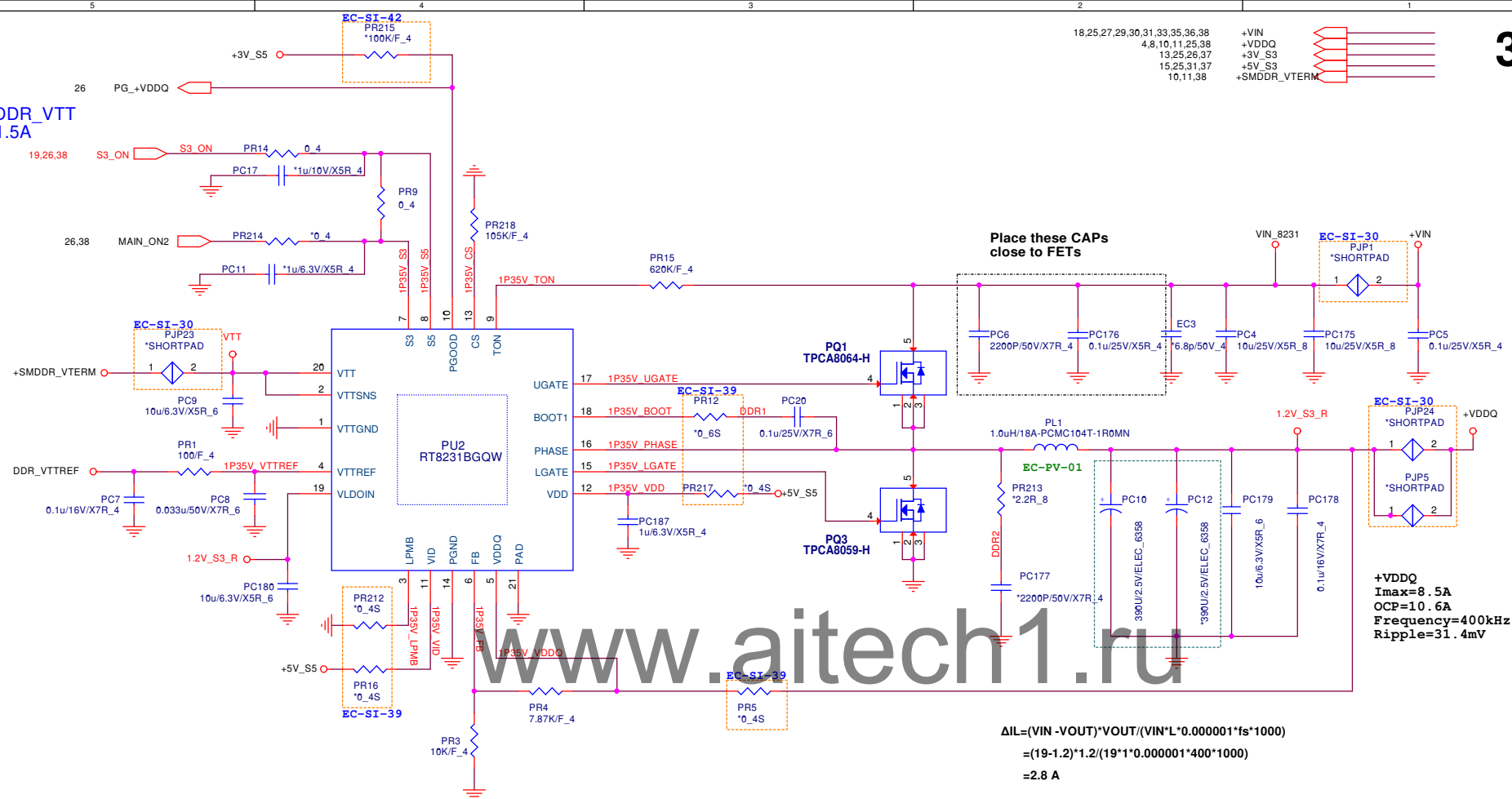


18,25,27,29,30,31,33,35,36,38
4,8,10,11,25,38
13,25,26,37
15,25,31,37
10,11,38

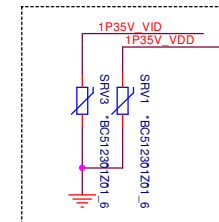
+VIN
+VDDQ
+3V_S3
+5V_S3
+SMDRR_VTERM



+0.6V_DDR_VTT
PEAK:1.5A



ESD reserve



Quanta Computer Inc.
PROJECT HP-PHUKET

Size	Document Number	Rev
--	VDDQ	C
Date:	Wednesday, January 27, 2016	Sheet 34 of 44

[illegible]

+1.5V

+1.5V VIN

+3V_S5

+1.5V_PG

+1.5V_P

+1.5V

IMAX= 0.2A

Pd= 0.06W

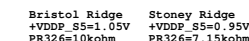
Vout = 0.8 (1+R1/R2)

$$\begin{aligned}\Delta I_L &= (V_{IN} - V_{OUT}) \cdot V_{OUT} / (V_{IN} \cdot L \cdot 0.000001 \cdot f_s \cdot 1000) \\ &= (3.3 - 1.8) \cdot 1.8 / 3.3 \cdot 1 \cdot 0.000001 \cdot 1000 \cdot 1000 \\ &= 0.72 \text{ A}\end{aligned}$$

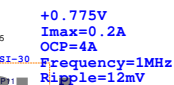
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$$V_{out} = 0.925 * ((R1 + R2) / R2)$$

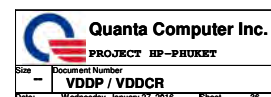
$$\begin{aligned}\Delta I_L &= (V_{IN} - V_{OUT}) \cdot V_{OUT} / (V_{IN} \cdot L \cdot 0.000001 \cdot f_s \cdot 1000) \\ &= (19 - 12) \cdot 12 / (19 \cdot 6.8 \cdot 0.000001 \cdot 357 \cdot 1000) \\ &= 1.82A\end{aligned}$$



$$\begin{aligned}\Delta I_L &= (V_{IN} - V_{OUT}) \cdot V_{OUT} / (V_{IN} \cdot L \cdot 0.000001 \cdot f_s \cdot 1000) \\ &= (19 - 1.05) \cdot 5 / (19 \cdot 1 \cdot 0.000001 \cdot 500 \cdot 1000) \\ &= 3.3 \text{ A}\end{aligned}$$



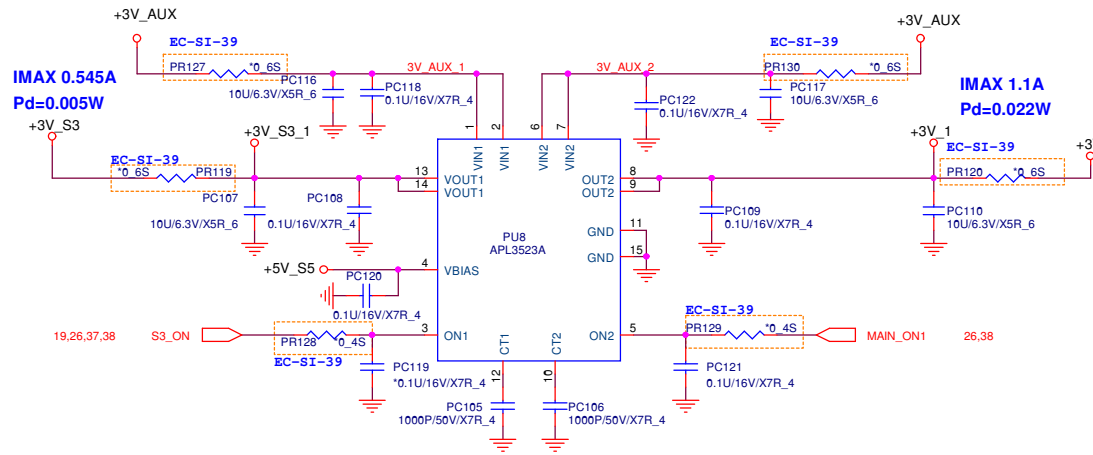
$$\begin{aligned}\Delta I_L &= (V_{IN} - V_{OUT}) \cdot V_{OUT} / (V_{IN} \cdot L \cdot 0.000001 \cdot f_s \cdot 1000) \\ &= (3.3 - 0.775) \cdot 0.775 / (3.3 \cdot 1 \cdot 0.000001 \cdot 1000 \cdot 1000) \\ &= 0.59 \text{ A}\end{aligned}$$



Load Switch

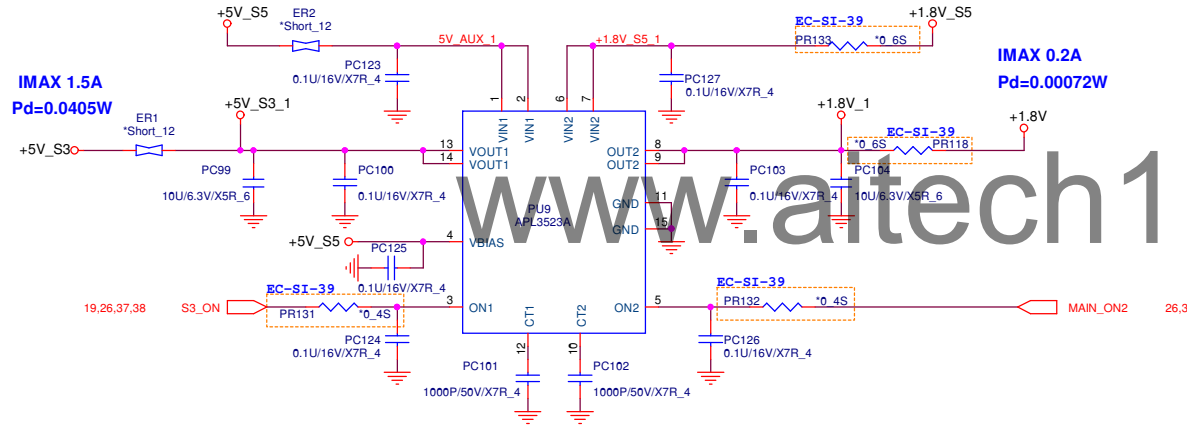
APL3523A
Channel 1 Rds(on)=18ohm
Channel 2 Rds(on)=18ohm

IMAX 0.545A
Pd=0.005W

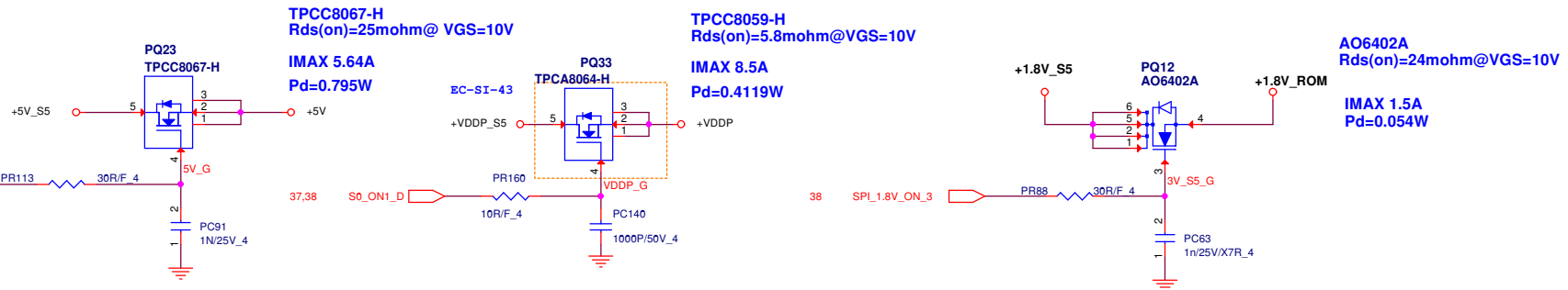


18,27	+5V_ALW
15,18,25,31	+5V_S3
13,25,26	+3V_S3
13,14,15,18,23,25,31,38	+5V
5,6,7,8,10,11,12,14,15,16,17,18,22,23,24,26,28	+3V
6,8,26,35,38	+1.8V_S5
3,5,6,7,15,26,28,32	+1.8V
8,15,35,38	+1.5V
7,8,36,38	+VDDP_S5
3,7,8,26,38	+VDDP
19,20,23,25,27,28,32,34,35,36	+5V_S5
6,7,8,16,19,21,25,26,27,32,34,35,36	+3V_S5

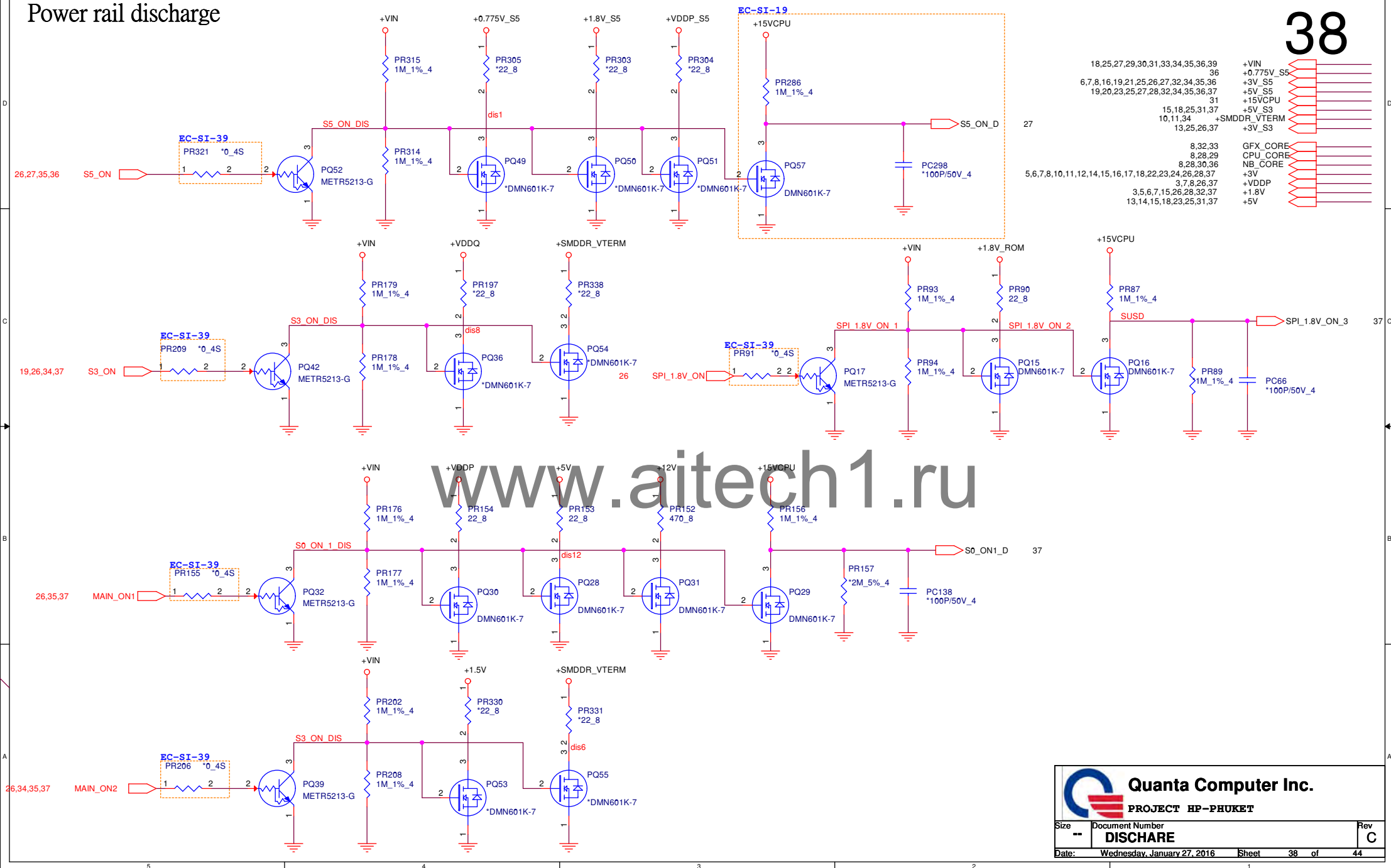
37



S0 ON_1 Load SW



Power rail discharge

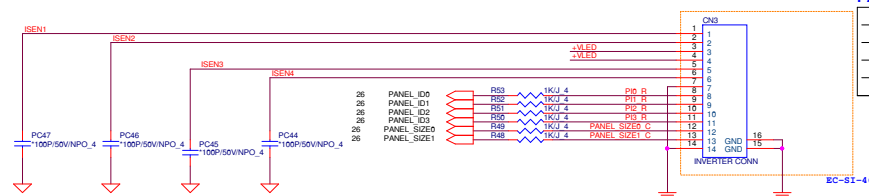


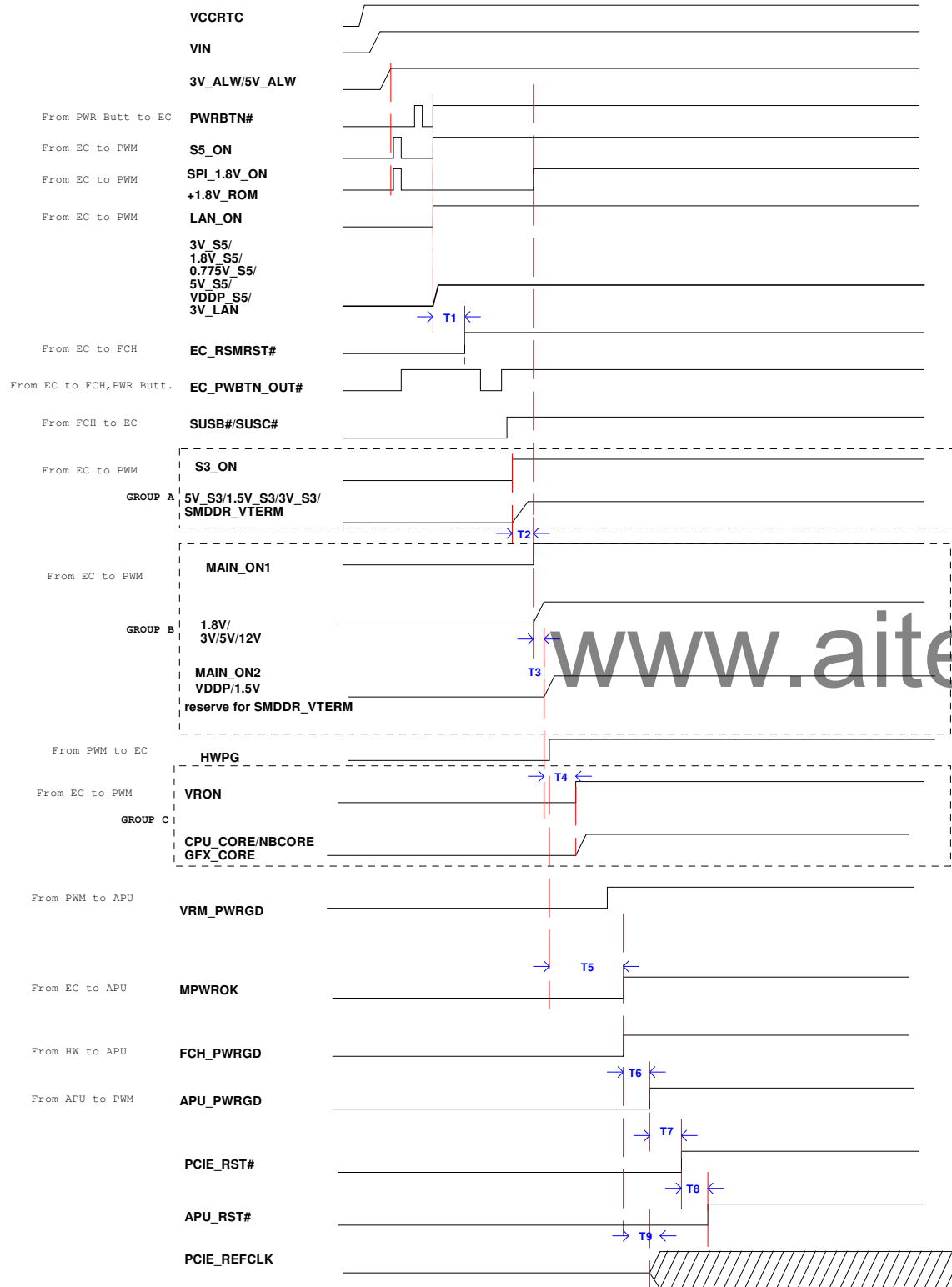


PANEL_ID[3:0]	Panel model
1111	No Connect
1110	AVL1
1101	AVL2
1100	AVL3
1011	AVL4
1010	AVL5
1001	Reserve
1000	Reserve

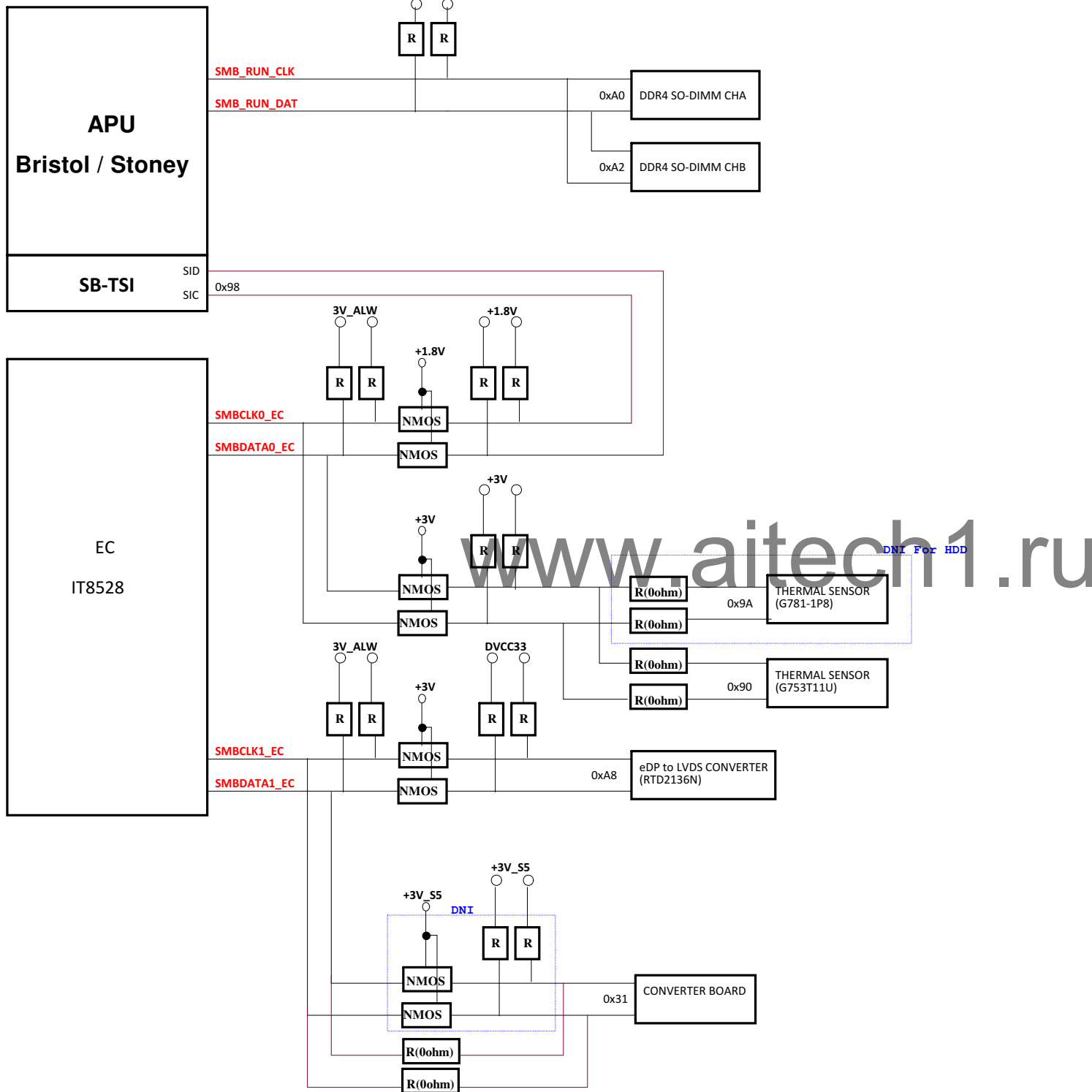
PANEL_ID[3:0]	Panel model
1111	No Connect
1110	AVL1
1101	AVL2
1100	AVL3
1011	AVL4
1010	AVL5
1001	Reserve
1000	Reserve

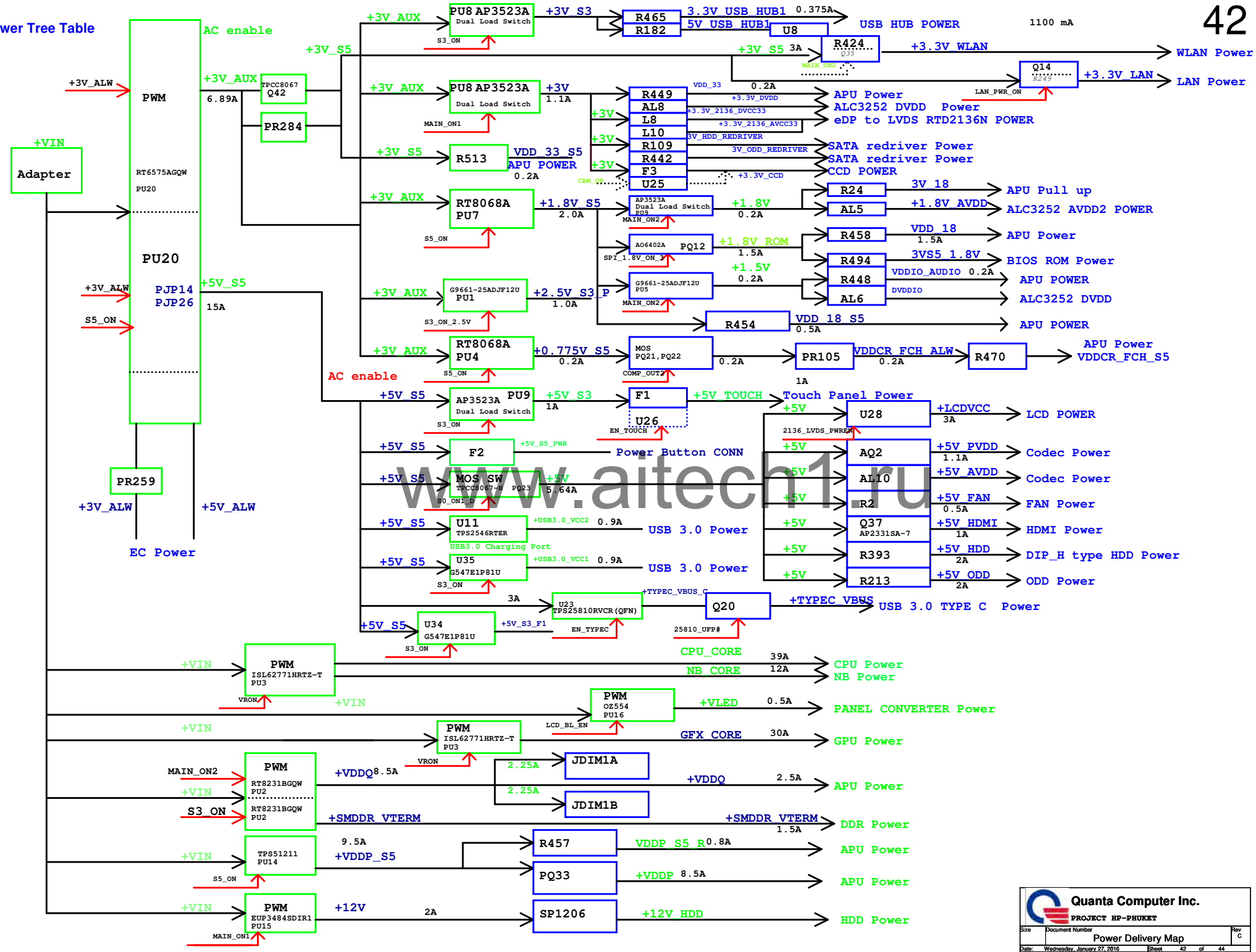
PANEL_Size[1:0]	Size
00	TBD
01	23.8"
10	27"
11	*No Connection





System Power Sequence	
EC Control:	
T1: S5_ON TO EC_RSMRST#	± 20ms
T2: S3_ON TO S0_ON1	± 10ms
T3: S0_ON1 TO S0_ON2	± 1ms
T4: S0_ON2 TO VRON	± 10ms
T5: HWPG TO MPWROK	± 99ms
Timing spec:	
T1 Spec:	10ms min
Power Up Spec:	
Group A > Group B > Group C	
T6: FCH_PWRGD TO APU_PWRGD	± 108.6 - 118.6 ms
T7: APU_PWRGD TO PCIE_RST#	± 114.2 - 124.2 ms
T8: PCIE_RST# TO APU_RST#	± 111.9 - 121.9 ms
T9: FCH_PWRGD TO PCIE_REFCLK	± 37.6 - 47.6 ms





EC #	Page	Description	Part Affected
EC-SI-01	31	Change PR163 to 45.3K ohm (CS34532FB18) from 60.4Kohm(CS36042FB10) for Stoney 25W.	PR163
EC-SI-02	26	Add R553 and R554 for Product_ID.	R553, R554
EC-SI-03	15	Change AL12 and AL14 to BEAD (CX8SG121000) from BEB(CX11B121007) for Vendor suggestion.	AL12,AL14
EC-SI-04	6	Change C37 and C38 to 15pF (CH01506JB06) from 18pF(CH01806JB07) for timer adjust.	C37,C38
EC-SI-05	7	Change R67 and R68 to 33 ohm (CS03302JB29) from 0 ohm(CS00002JB38) for EA test resule.	R67,R68
EC-SI-06	26	Add R561 ~ R564 for Second FAN control.	R562,R564
EC-SI-07	23	Add R565,R566,R567,C456,C457,EC65,EC66 and CN25 foSecond FAN reserved.	
EC-SI-08	23	Change H5 FT change to "spad-re394x315" from "H-SAFAN-2-N83" for Second FAN reserved.	
EC-SI-09	15	Add CAM_ON of GPIO for DMIC icon disable.	
EC-SI-10	18	CN2 pin 5 (CAM ON) and pin 9 (IR ON) remove for IR / WEB CAM change	
EC-SI-11	16	Add R469 0 ohm, Stuff C438 and C420 0.1uF for EMI.	R469,C438,C420
EC-SI-12	15	Stuff AR5,AC23 and AR28 0.1uF for EMI.	AR5,AC23,AR28
EC-SI-13	18	Stuff D3,D4,D5,D6,D15,U1 and U2 for ESD.	D3,D4,D5,D6D15,U1,U2
EC-SI-14	10	Change C179 to D45 for ESD.	C179,D45
EC-SI-15	11	Change C188 to D46 for ESD.	C188,D46
EC-SI-16	32	Change PC32 to 150pF (CH11506JB08) from 100pF(CH1106JB00) for transient adjust for Bristol 35W.	PC32
EC-SI-17	32	Change PR44 to 32.4K ohm (CS33242FB19) from 2K ohm(CS22002FB19) for transient adjust for Bristol 35W.	PR44
EC-SI-18	28	Change PR268 to 68K ohm (CS36802FB00) from 137K ohm(CS41372FB12) for loopgain for Stoney 25W.	PR268
EC-SI-19	27	Add Q42,R570,C459,PR342,PR317 and PR320 for +3V_AUX	Q42,R570,C459,PR342,PR317,PR320
EC-SI-20	27	Reserve PR284,PR312 and PR302 for +3V_S5	
EC-SI-21	19	Add R568,R569 and change R236,R217,R221 power rail for +3V_S5 or +3V_AUX option	R568,
EC-SI-22	19	U34,U35 change to G5248 from G547E1	U34,U35
EC-SI-23	19	Del C116 and C115 change to 330uF from 150uF	C115
EC-SI-24	6	Del D24 and D28 change to BAT54AW from RB500V	D28
EC-SI-25	3, 6	Add D47,D48,D50 ~D54 TVS AZ5123-01H for ESD	D47,D48,D50,D51
EC-SI-26	6	Unstuff R425 and Stuff R431 10K ohm for Board ID change	R431
EC-SI-27	8	Del D1 and D2 change to BAT54CW from RB500V	D2
EC-SI-28	14	Del D12 and D13 change to BAT54AW from RB500V	D13
EC-SI-29	14	Q37 AP2331SA change to F5 Poly Fuse 1A/5V	F5
EC-SI-30	27,29,30,33,34,35,36,39	PJP17,PJP18,PJP14,PJP20,PJP25,PJP8,PJP9,PJP6,PJP2,JP1,PJP24,PJP5,PJP16,PJP10,PJP13,PJP22,PJP19,PJP28,PJP7 change to Short PAD	
EC-SI-31	26	D23,D31,D33 change to 0 ohm(R571,R573,R574) from 0 ohm B0530WS. EC pin swap for OPB second FAN.	
EC-SI-32	12	C79 and C397 change to 10uF from 22uF	
EC-SI-33	14	Del Q13 and Q12 change to 2N7002KDW Dual from PJA18K	
EC-SI-34	17	C419,C424 and C111 change to 4.7uF/6.3V from 4.7uF/10V	
EC-SI-35	18	C162 and C166 change to 1uF/6.3V from 4.7uF/10V	
EC-SI-36	21	C31 and C36 change to 4.7uF/6.3V from 10uF/6.3V	
EC-SI-37	20,23	Unstuff C144,C145 10uF/6.3V and C95 22uF/10V	
EC-SI-38	26	Reserve R579 (180ohm) and R388 (150ohm) for EC_FSP pin Alway power rail	
EC-SI-39		Change AR9,R1,R2,SR1~SR13,R24,R34,R35,R36,R39,R81,B3,R136,R324,R348,R394,R405,R422,R448,R449,R477,R494,R360 to short pad from 0 ohm	
EC-SI-40	26	Change D29,D25,D16,D22,D19,D17,D8 to 0ohm(R581~R587)from 1SS355	
EC-SI-41	22,4	Stuff R103,R105 : 4.7K ohm. Unstuff R313,R312,C17C176	
EC-SI-42	27,34,35	PR2,PR96, PR215, PR320, PR191, PR121no mount	
EC-SI-43	37	PQ33 change to TPCA8064 from TPCA8059	
EC-SI-44	16,20,39	CN18, CN23, CN3 change new P/N & FP for SMT	CN18, CN23, CN3
EC-SI-45	22	Stuff R101	R101
EC-SI-46	14,39	CN3: DFHD14MR054 to DFHD14MS102(old EOL);L14: DC0904A014 to CX900T04000(old EOL)	CN3,L14
EC-SI-47	29,30,33	CPU 1. PR248 & PR265 changed to 0 ohm from 2.2 ohm. 2.Delete PR229,PC207 and PR262 and PC241. NB. 1. PR269 changed to 0 ohm from 2.2 ohm.2.Delete PR282&PC257 GFX 3. PR23 & PR35 changed to 0 ohm from 2.2 ohm. 4. Delete PR222,PC190 and PR220 and PC188.	PR248,PR265,PR229,PC207,PR262,PC241. PR269,PR282,PC257,PR23,PR35 PR222,PC190,PR220,PC188.
EC-SI-48	22,23	Stuff R138,R144,R156,R158 : 0 ohm. C73,C78,C85,C88,0.01uF. Unstuff C50,C54,C63,C65,C72,C77,C84,C88	R138,R144,R156,R158,C73,C78,C85,C89, C50,C54,C63,C65,C72,C77,C84,C88
EC-SI-49	28,29	Stoney 15W Stuff PR67,PR68,PQ56. Unstuff PC52,PC53,PC251,PC61,PC250,PC249,PC60,PC43,PR230,PC228,PC229,PR265,PC239. PC230,PC231,PR61,PR62,PC216,PC227,PO9,PO10,PL5 Change the PR66 from 2.15K to 1.69K. CS21692FB01 ES CHIP 1.69K 1/16W +-1%(0402) Change the PC217 to 0.022uF CH3224K1B01 CAP CHIP 0.022uF 25V(+/-10%,XSR,0402) Change the PR239 from 392 to 487 CS14872FB05 RES CHIP 487 1/16W +-1%(0402)	PR67,PR68,PC52,PC53 PC52,PC53,PC251,PC61,PC250,PC249,PC60,PC43,PR230,PC228,PC229 PR66,PR239,PC217.

EC #	Page	Description	Part Affected
EC-PV-01	34	Pop PC10 and non pop PC12 for QCMC request.	
EC-PV-02	29	CPU 2nd phase FET be H1L2 for lmax efficiency.	
EC-PV-03	24	Add EC67 ~ EC82 0.1uF and EC83 ~ EC87 82pF for EMI.	
EC-PV-04	26	D27 change to 0 ohm(R575) from Diode B0530WS.	
EC-PV-05	6	Unstuff R163,R431 and Stuff R149,R425 10K ohm for Bard ID change	
EC-PV-06	6	Delete R394 and R348 Change to 0 ohm from short PAD	
EC-PV-07	6	Stuff C16 and C21 10pF for EMI.	
EC-PV-08	25	Stuff EC48,EC52,EC59,EC61,EC53,EC55,EC1,EC2,EC6,EC8,EC9,EC42,EC60,EC35 0.1uF and C36,EC37,EC38,EC39,EC40,EC44,EC45 82pF for EMI.	
EC-PV-09	28	Remove PC254 & PR272 for Stardust dynamic test	
EC-PV-10	28	Add Change PR232 to 41.2 K ohm for Stardst dynamic test	
EC-PV-11	29	CPU_CORE Add PC302 330U*1 + PC299&PC300 70U* 2 for Stardust dynamic test	
EC-PV-12	30	NB_CORE Add PC301 330U*1 & delete PC261&C262 22U*2 for or Stardust dynamic test	
EC-PV-13	08	CPU_CORE Changed from C232,C233,C257,C22,C273,C234,C255,C270,C256 22U*9 to 47U*9 ADD C462,C461,C460,C458 47U*4 for or Stardust dynatic test	
EC-PV-14	08	NB_CORE CPU_CORE Changed from C346,C38,C345,C344 22U*4 to 47U*4 ADD C463 47U*1 for or Stardust dynamic test	22U*2 for or Stardust dynamic test
EC-PV-15	18	Reserve F6 for Touch power	
EC-PV-16	25	Change H14 FT to "h-tc236ic126bc126d126pttfrom "h-tc122ic122bc236d122pb".	
EC-PV-17	23	U3 change to G753 from G781-1, Delete Q4,C8,R69.	
EC-PV-18	23	U18 change to G781-1 from G753, Add C110&394.	
EC-PV-19	15	Change AL11 and AL13 to BEAD (FCM1005KF-121T03_300A_4) from BEAD(CX11B121007)	

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